MoSys, Inc.
Form S-1/A
January 25, 2018
Table of Contents

As filed with the Securities and Exchange Commission on January 25, 2018

Registration No. 333-222417

UNITED STATES

SECURITIES AND EXCHANGE COMMISSION

WASHINGTON, D.C. 20549

AMENDMENT NO. 1

TO

FORM S-1

REGISTRATION STATEMENT

UNDER

THE SECURITIES ACT OF 1933

MOSYS, INC.

(Exact name of registrant as specified in its charter)

Delaware	3674	77-0291941
(State or other jurisdiction of incorporation or organization)	(Primary Standard Industrial Classification	(I.R.S. Employer Identification No.)

Code Number)

2309 Bering Drive

San Jose, California 95131

(408) 418-7500

(Address, including zip code, and telephone number, including area code, of registrant's principal executive offices)

Leonard Perham

Chief Executive Officer and President

MoSys, Inc.

2309 Bering Drive

San Jose, CA 95131

(408) 418 7500

(Name, address, including zip code, and telephone number, including area code, of agent for service)

Copies of all communications to:

Alan B. Kalin

Pillsbury Winthrop Shaw Pittman LLP

2550 Hanover Street

Palo Alto, CA 94304

(650) 233-4048

Approximate date of commencement of proposed sale to the public:

From time to time after this registration statement is declared effective.

If any of the securities being registered on this Form are to be offered on a delayed or continuous basis pursuant to Rule 415 under the Securities Act of 1933, check the following box.

If this Form is filed to register additional securities for an offering pursuant to Rule 462(b) under the Securities Act, please check the following box and list the Securities Act registration statement number of the earlier effective registration statement for the same offering.

Table of Contents

If this Form is a post-effective amendment filed pursuant to Rule 462(c) under the Securities Act, check the following box and list the Securities Act registration statement number of the earlier effective registration statement for the same offering.

If this Form is a post-effective amendment filed pursuant to Rule 462(d) under the Securities Act, check the following box and list the Securities Act registration statement number of the earlier effective registration statement for the same offering.

Indicate by check mark whether the registrant is a large accelerated filer, an accelerated filer, a non-accelerated filer, or a smaller reporting company. See the definitions of “large accelerated filer,” “accelerated filer” and “smaller reporting company” in Rule 12b-2 of the Exchange Act. (Check one):

Large Accelerated filer	Accelerated filer	Non-accelerated Filer (Do not check if a smaller reporting company)
Smaller reporting company	Emerging growth company	

If an emerging growth company, indicate by check mark if the registrant has elected not to use the extended transition period for complying with any new or revised financial accounting standards provided pursuant to Section 13(a) of the Exchange Act.

CALCULATION OF REGISTRATION FEE

Title of each class of securities to be registered	Amount To be Registered	Proposed maximum offering price per share (1)	Proposed maximum aggregate offering price	Amount of registration fee(2)
	662,500	$2.35	$1,556,875	193.83

Common Stock, par value $0.001 per share,
underlying common stock purchase warrants

(1) Calculated pursuant to Rule 457(c) and (h)(1) of the regulations under the Securities Act of 1933, as amended (the "Securities Act") based on the price at which the warrants may be exercised.

(2) Calculated pursuant to Rule 457(o) of the regulations under the Securities Act of 1933.

The registrant hereby amends this registration statement on such date or dates as may be necessary to delay its effective date until the registrant shall file a further amendment which specifically states that this registration statement shall thereafter become effective in accordance with Section 8(a) of the Securities Act of 1933, as amended, or until the registration statement shall become effective on such date as the Securities and Exchange Commission, acting pursuant to said Section 8(a), may determine.

Table of Contents

The information in this prospectus is not complete and may be changed. The selling stockholders may not sell these securities pursuant to this prospectus until the registration statement filed with the Securities and Exchange Commission is effective. This prospectus is not an offer to sell these securities and is not soliciting offers to buy these securities in any jurisdiction where the offer or sale is not permitted.

SUBJECT TO COMPLETION, DATED JANUARY 25, 2018

PROSPECTUS

662,500 Shares of Common Stock

Issuable upon Exercise of Outstanding Warrants

This prospectus relates to the resale, from time to time, by the selling stockholders identified in this prospectus under the caption “Selling Stockholders,” of up to 662,500 shares of our common stock, par value $0.001 per share, issuable upon exercise of outstanding common stock purchase warrants issued in a private placement transaction on July 6, 2017. We are not selling any shares of common stock under this prospectus and will not receive any proceeds from the sale of shares of common stock by the selling stockholders. We will receive proceeds from the cash exercise of the warrants, which, if exercised in cash with respect to all of the 662,500 shares of common stock, would result in gross proceeds of approximately $1,556,875 to us before commissions and expenses. The selling stockholders will bear all commissions and discounts, if any, attributable to the resale of the shares.

The selling stockholders may sell the shares of our common stock offered by this prospectus from time to time on terms to be determined at the time of sale through ordinary brokerage transactions or through any other means described in this prospectus under the caption “Plan of Distribution.” The shares of common stock may be sold at fixed prices, at market prices prevailing at the time of sale, at prices related to prevailing market price or at negotiated prices.

Our common stock is listed on The NASDAQ Capital Market under the symbol “MOSY.” On January 24, 2018, the last reported closing sale price of our common stock on The NASDAQ Capital Market was $1.36 per share.

INVESTING IN OUR SECURITIES INVOLVES RISKS.

SEE “RISK FACTORS” ON PAGE 6.

Neither the Securities and Exchange Commission nor any state securities commission has approved or disapproved of these securities or determined if this prospectus is truthful or complete. Any representation to the contrary is a criminal offense.

The date of this prospectus is January , 2018.

Table of Contents

TABLE OF CONTENTS

In this prospectus, "MoSys," "we," "us," and "our" refer to MoSys, Inc. and its subsidiaries.

You should rely only on information contained or incorporated by reference in this prospectus. We have not authorized any person to provide you with information that differs from what is contained or incorporated by reference in this prospectus. If any person does provide you with information that differs from what is contained or incorporated by reference in this prospectus, you should not rely on it. This prospectus is not an offer to sell or the solicitation of an offer to buy any securities other than the securities to which it relates, or an offer of solicitation in any jurisdiction where offers or sales are not permitted. The information contained in this prospectus is accurate only as of the date of this prospectus, even though this prospectus may be delivered or shares may be sold under this prospectus on a later date.

Table of Contents

ABOUT THIS PROSPECTUS

This prospectus relates to the resale by the selling stockholders identified in this prospectus under the caption “Selling Stockholders,” from time to time, of up to 662,500 shares of our comment stock, par value $0.001 per share, issuable upon exercise of outstanding common stock purchase warrants, or the warrants, issued in a private placement transaction on July 6, 2017. On January 6, 2018, 662,500 shares of common stock became exercisable by the selling stockholders. We are not selling any shares of common stock under this prospectus and will not receive any proceeds from the sale of shares of common stock by the selling stockholders.

This prospectus is part of a registration statement on Form S 1 that we filed with the Securities and Exchange Commission, or SEC. It omits some of the information contained in the registration statement and reference is made to the registration statement, as well as other documents we have filed with the SEC, for further information with regard to us and the securities being offered by the selling stockholders. Any statement contained in the prospectus concerning the provisions of any document filed as an exhibit to the registration statement or otherwise filed with the SEC is not necessarily complete, and in each instance, reference is made to the copy of the document filed.

You should read this prospectus, any documents that we incorporate by reference in this prospectus and the registration statement, and the additional information described below under “Where You Can Find Additional Information” and “Information Incorporated by Reference” before making an investment decision.

FORWARD-LOOKING STATEMENTS

Some of the statements in this prospectus constitute forward-looking statements. These statements involve known and unknown risks, uncertainties, and other factors that may cause our or our industry’s actual results, levels of activity, performance, or achievements to be materially different from any future results, levels of activity, performance, or achievements expressed or implied by such forward-looking statements. These factors include, among others, those incorporated by reference under “Risk Factors” below.

In some cases, you can identify forward-looking statements by terms such as “may,” “will,” “should,” “expects,” “plans,” “anticipates,” “believes,” “estimates,” “predicts,” “potential,” or “continue” or similar terms.

Although we believe that the expectations reflected in the forward-looking statements are reasonable, we cannot guarantee future results, levels of activity, performance, or achievements. Our actual results could differ materially from those expressed or implied by these forward-looking statements as a result of various factors, including the risk factors incorporated by reference under the heading “Risk Factors” below and a variety of other factors, including, without limitation, statements about our future business operations and results, the market for our technology, our strategy and competition.

Moreover, neither we nor any other person assumes responsibility for the accuracy and completeness of these statements. We undertake no obligation to update or revise any of the forward-looking statements, whether as a result of new information, future events or otherwise, except as required by law. In light of these risks, uncertainties and assumptions, the forward-looking events discussed or incorporated by reference in this prospectus may not occur.

Table of Contents

PROSPECTUS SUMMARY

The following summary highlights information contained elsewhere or incorporated by reference in this prospectus. This summary does not contain all of the information you should consider before investing in the securities. Before making an investment decision, you should read the entire prospectus carefully, including the matters discussed under the heading “Risk Factors” in this prospectus.

Our Company

We are a fabless semiconductor company focused on the development and sale of integrated circuits, or ICs, for the high-speed networking, communications, storage and data center markets. Our solutions deliver time-to-market, performance, power, area and economic benefits for system original equipment manufacturers, or OEMs. Our principal product line and source of substantially all of our revenue is the Bandwidth Engine® product family. Bandwidth Engine ICs combine our proprietary 1T-SRAM® high-density embedded memory, integrated macro functions and high-speed serial interface, or SerDes, I/O, with our intelligent access technology and a highly efficient interface protocol. Historically, our primary business was the design, development, marketing, sale and support of differentiated intellectual property, or IP, including embedded memory and high-speed parallel and SerDes I/O used in advanced systems-on-chips, or SoCs.

Our future success and ability to achieve and maintain profitability are dependent on the marketing and sales of our Bandwidth Engine IC products into networking, communications and other markets requiring high-bandwidth memory access.

We incurred a net loss of $10.1 million for the nine month period ended September 30, 2017 and had an accumulated deficit of $224.2 million as of September 30, 2017. In addition, we incurred net losses of approximately $32.0 million and $31.5 million for the years ended December 31, 2016 and 2015, respectively. These and prior year losses have resulted in significant negative cash flows for almost a decade and have required us to raise substantial amounts of additional capital during this period. To date, we have primarily financed our operations through multiple offerings of common stock to investors and affiliates, as well as asset sale transactions.

In March 2016, we entered into a 10% Senior Secured Convertible Note Purchase Agreement with the purchasers of $8.0 million principal amount of 10% Senior Secured Convertible Notes due August 15, 2018 (the "Notes"), at par, in a private placement transaction. The Notes bear interest at the annual rate of 10%. Accrued interest is payable semi-annually in cash or in-kind through the issuance of identical new Notes, or with a combination of the two, at our option. Since issuance of the Notes, we have made the interest payments in-kind through the issuance of additional notes totaling approximately $1.2 million. Further, the Notes restrict our ability to incur any indebtedness for borrowed money, unless such indebtedness by its terms is expressly subordinated to the Notes in right of payment and to the security interest of the Note holder(s) in respect to the priority and enforcement of any security interest in our property securing such new debt; provided that the Note holder(s) security interest and cash payment rights under the Notes shall be subordinate to a maximum of $5 million of indebtedness for a secured accounts receivable line of credit facility under certain conditions.

We expect to continue to incur operating losses for the foreseeable future as we secure customers for and continue to invest in the commercialization of our Bandwidth Engine IC products. We will need to increase revenues substantially beyond levels that we have attained in the past in order to generate sustainable operating profit and sufficient cash flows to continue doing business without raising additional capital from time to time. As a result of our expected operating losses and cash burn for the foreseeable future, recurring losses from operations, and the need to repay the Notes and accrued interest in 2018, if we are unable to raise sufficient capital through additional debt or equity arrangements, there will be uncertainty regarding our ability to maintain liquidity sufficient to operate our business

effectively, which raises substantial doubt as to our ability to continue as a going concern. There can be no assurance that such additional capital, whether in the form of debt or equity financing, will be sufficient or available and, if available, that such capital will be offered on terms and conditions acceptable to us. We are primarily focusing our resources on producing and selling our existing products, and have substantially curtailed new product development. If we are unsuccessful in these efforts, we will need to implement additional cost reduction strategies, which could further affect our near- and long-term business plan. These efforts may include, but are not limited to, further reducing headcount and curtailing business activities.

Table of Contents

The address and phone number of our principal executive offices are MoSys, Inc., 2309 Bering Drive, San Jose, CA 95131, (408) 418 7500.

Our Strategy

Our primary business objective is to be an IP-rich fabless semiconductor company offering ICs that deliver unparalleled bandwidth performance for next generation data center, networking and communications systems.

Our Business

Bandwidth Engine

The Bandwidth Engine is a memory-dominated IC that has been designed to be a high-performance companion IC to packet processors. While the Bandwidth Engine primarily functions as a memory device with a high-performance and high-efficiency interface, it also can accelerate certain processing operations by serving as a co-processor element. Our Bandwidth Engine ICs combine: (1) our proprietary high-density, high-speed, low latency embedded memory, (2) our SerDes, (3) an open-standard interface protocol and (4) intelligent access technology. We believe an IC combining our 1T-SRAM memory and serial I/O with logic and other intelligence functions provides a system-level solution and significantly improves overall system performance at lower cost, size and power consumption. Our Bandwidth Engine ICs can provide up to and over 4.5 billion memory accesses per second, which is more than twice the performance of current memory-based solutions. They also can enable system designers to significantly narrow the gap between processor and memory IC performance. Customers that design Bandwidth Engine ICs onto the line cards in their networking systems will re-architect their systems at the line-card level and use our product to replace traditional memory solutions. When compared with existing commercially available solutions, our Bandwidth Engine ICs may:

- provide up to four times the performance;
- reduce power by approximately 50%;
- reduce cost by greater than 50%; and
- result in a dramatic reduction in IC pin counts on the line card.

Our first generation Bandwidth Engine IC, or BE1, products contain 576 megabytes, or MB, of memory and use a serial I/O with up to 16 lanes operating at up to 10.3 Gbps per lane. Variations of the BE1 can have up to two interface ports, with up to eight serial receiver and eight serial transmitter lanes per port for a total of 16 lanes of 10.3 Gbps SerDes interface. These ICs include an arithmetic logic unit, which can perform read-modify-write operations. We have been shipping our BE1 products since 2012. We have notified customers, however, that we intend to discontinue our BE1 products. We expect to complete final shipments of our BE1 products by the end of 2018.

Our second generation Bandwidth Engine IC, BE2, products contain 576 MB of memory and use serial I/O with up to 16 lanes operating at up to 15 Gbps per lane. In addition to a speed improvement of up to 50%, the architecture enables several family member parts with added specialized features. To date, we have announced three unique devices in this product family:

- MSR620 with burst features optimized for oversubscription buffer applications;
- MSR720 with a write cache and memory coherency capability that allows for deterministic look-ups optimized for state and queue type applications; and
- MSR820 with increased intelligence for lookup, metering and statistics applications by adding dual counters, atomic and extensive metering functions.

Table of Contents

We have been shipping our BE2 products since 2013. These products represented the majority of our revenues in 2016. We expect our BE2 products to represent the majority of our revenues for the foreseeable future.

Our third generation Bandwidth Engine IC, or BE3, products contain 1152 MB of memory and use serial I/O with up to 16 lanes operating at up to 30 Gbps per lane. BE3 targets support for packet-processing applications with up to five billion memory single word accesses per second, as well as burst mode to enable full duplex buffering up to 400Gbps for ingress, egress and oversubscription applications. To date, we have announced three unique devices in this product family:

- MSR630 enables high rate lookup or high-performance buffer capabilities; and
- MSR830 offers additional offload capabilities for functions such as statistics and metering to increase performance and add features for next-generation networking and communications equipment; and
- MSRZ30 builds upon the capabilities and performance of the MSR830, with data rates, interface protocol and data structures that are optimized for the EZchip NPS 400 network processing unit, or NPU, and can increase memory bandwidth by up to 50%.

We commenced sampling of our BE3 products in 2016, and expect to qualify these products for mass production in the first half of 2018. We do not have a current estimate of the timing for significant revenues from our BE3 products.

IP Licensing and Distribution

Historically, we offered our memory and I/O technologies on a worldwide basis to semiconductor companies, electronic product manufacturers, foundries, intellectual property companies and design companies through product development, technology licensing and joint marketing relationships. We licensed our IP technology to semiconductor companies who incorporated our technology into ICs that they sold to their customers. As a result of the change in our corporate strategy, since early 2012, our IP licensing activities have been limited, and we expect this to continue. However, for the nine months ended September 30, 2017 and the year ended December 31, 2016, approximately 15% and 24%, respectively, of our total revenues were generated from licensing and royalties related to our existing licensing arrangements, as we continued to perform and deliver under outstanding license agreements and collect royalties from 1T- SRAM licensees. To date, we have completed our performance obligations under our existing licensing agreements, and we expect licensing and royalty revenues to be minimal in future years.

Description of the Private Placement of Warrants

On June 30, 2017, we entered into a Securities Purchase Agreement (the “Purchase Agreement”), with participating investors, who are the selling stockholders identified in this prospectus under the caption “Selling Stockholders,” pursuant to which we sold and issued, in a registered direct offering, an aggregate of 1,325,000 shares of our common stock at an offering price of $1.70 per share (the “Shares”) on July 6, 2017. In addition, pursuant to the Purchase Agreement, we agreed to sell and issue a warrant to purchase one half of a share of the common stock for each share purchased for cash in the offering pursuant to Common Stock Purchase Warrants, or the warrants, to purchase 662,500 shares of our common stock.

The warrants have an exercise price of $2.35 per share of our common stock, may be exercised from time to time beginning January 6, 2018 (the “Initial Exercise Date”), and at any time thereafter up to the date that is five years from the date when first exercisable, at which time any unexercised warrants will expire and cease to be exercisable. The warrants will be exercisable, at the option of each holder, in whole or in part by delivering to us a duly executed exercise notice and by payment in full in immediately available funds for the number of shares of common stock purchased upon such exercise. If a registration statement registering the issuance of the shares of common stock underlying the warrants under the Securities Act is not then effective or available, the holder may exercise the warrant through a cashless exercise, in whole or in part, in which case the holder would receive upon such exercise the net

number of shares of common stock determined according to the formula set forth in the warrant. No fractional shares of common stock will be issued in connection with the exercise of a warrant. In lieu of fractional shares, we will either pay the holder an amount in cash equal to the fractional amount multiplied by the exercise price or round up to the next whole share.

Table of Contents

A holder will not have the right to exercise any portion of the warrant if the holder (together with its affiliates) would beneficially own in excess of 4.99% (or on election of the holder, 9.99%) of the number of shares of our stock outstanding immediately after giving effect to the exercise, as such percentage ownership is determined in accordance with the terms of the warrants. However, any holder may increase or decrease such percentage to any other percentage not in excess of 9.99% upon notice to us, provided that any increase in such percentage shall not be effective until 61 days after such notice to us.

The initial exercise price per share of common stock purchasable upon exercise of the warrants is $2.35 per share of common stock. The exercise price is subject to appropriate adjustment in the event of certain stock dividends and distributions, stock splits, stock combinations, reclassifications or similar events affecting our common stock.

In the event of a fundamental transaction, as described in the warrants, which generally includes any reorganization, recapitalization or reclassification of our common stock, the sale, transfer or other disposition of all or substantially all of our properties or assets, our consolidation or merger with or into another person, the holders of the warrants will be entitled to receive upon exercise of the warrants the kind and amount of securities, cash or other property that the holders would have received had they exercised the warrants immediately prior to such fundamental transaction.

We filed the registration statement on Form S 1, of which this prospectus is a part, to fulfill our obligation under the Purchase Agreement to provide for the resale by these investors of up to 662,500 shares of common stock issuable upon exercise of the warrants. We agreed to use commercially reasonable efforts to cause such registration statement to become effective 181 days following the date of issuance of the warrants (July 6, 2017) and to keep such registration statement effective at all times until (a) the warrant shares are sold under such registration statement or pursuant to Rule 144 under the Securities Act, (b) the warrant shares may be sold without volume or manner-of-sale restrictions pursuant to Rule 144 under the Securities Act, and (c) the five-year anniversary of the Initial Exercise Date, whichever is the earliest to occur.

The Offering

Shares of common stock offered by the selling stockholders:	662,500 shares of common stock issuable upon exercise of the outstanding common stock purchase warrants.
Shares of common stock outstanding before this offering:	8,067,635
Shares of common stock outstanding after completion of this offering, assuming full exercise of the common stock purchase warrants:	8,730,135
Terms of the Offering:	The selling stockholders, including their transferees, donees, pledgees, assignees and successors-in-interest, may sell, transfer or otherwise dispose of any or all of the shares of common stock offered by this prospectus from time to time on The NASDAQ Capital Market or any other stock exchange, market or trading facility on which the shares are traded or in private transactions. The shares of common stock may be sold at fixed prices, at market prices prevailing at the time of sale, at prices related to

prevailing market price or at negotiated prices.

Table of Contents

Use of Proceeds:	All proceeds from the sale of shares of common stock issuable upon exercise of the outstanding common stock purchase warrants will be for the account of the selling stockholders. We will not receive any proceeds from the sale of common stock offered pursuant to this prospectus. However, we will receive proceeds upon any cash exercise of the common stock purchase warrants. See the section titled “Use of Proceeds” in this prospectus.
NASDAQ Capital Market symbol:	MOSY
Trading:	Our shares of common stock currently trade on The NASDAQ Capital Market. There is no established trading market for the common stock purchase warrants and we do not intend to list the common stock purchase warrants on any exchange or other trading system.
Risk Factors:	Investing in our securities involves a high degree of risk and purchasers of our securities may lose their entire investment. See “Risk Factors” below and the other information included elsewhere in this prospectus for a discussion of factors you should carefully consider before deciding to invest in our securities.

The number of shares of our common stock shown above to be outstanding immediately before and after this offering is based on 8,067,635 shares outstanding as of December 31, 2017, and excludes, as of such date:

- 1,021,102 shares of common stock issuable upon conversion of the 10% Subordinate Senior Secured Convertible Notes due August 15, 2018;
- 72,759 shares of common stock issuable upon exercise of outstanding exercisable stock options with a weighted average exercise price of approximately $10.55 per share;
- 234,685 shares of common stock issuable upon exercise of outstanding stock options that are not exercisable;
- 376,490 shares of common stock issuable upon vesting of restricted stock units;
- 231,185 shares of common stock available for future issuance under our equity incentive plans;
- 147,024 shares of common stock available for sale under our employee stock purchase plan; and
- 662,500 shares of common stock issuable upon exercise of the warrants.

Table of Contents

RISK FACTORS

An investment in our common stock is risky. Prior to making a decision about investing in our common stock, you should carefully consider the specific risks discussed in this prospectus, any applicable prospectus supplement, or otherwise incorporated by reference in this prospectus. The risks and uncertainties described in our SEC filings are not the only ones facing us. Additional risks and uncertainties not presently known to us, or that we currently see as immaterial, may also harm our business. If any of the risks or uncertainties described in the prospectus supplement or our SEC filings or any such additional risks and uncertainties actually occur, our business, results of operations, cash flows and financial condition could be materially and adversely affected. In that case, the trading price of our common stock could decline, and you might lose part or all of your investment.

We have a history of losses and we will need to raise additional capital in the future and our inability to do so may adversely impact our ability to continue as a going concern.

Our consolidated financial statements have been prepared on a going concern basis that assumes we will be able to realize our assets and discharge our liabilities in the normal course of business for the foreseeable future. We incurred a net loss of $10.1 million for the nine-month period ended September 30, 2017, and had an accumulated deficit of $224.2 million as of September 30, 2017. We recorded an operating loss of approximately $31.4 million for the year ended December 31, 2016 and we ended the period with an accumulated deficit of approximately $214.0 million. In addition, we recorded operating losses of approximately $31.5 million and $32.7 million for the years ended December 31, 2015 and 2014, respectively. These losses have resulted in significant negative cash flows for more almost a decade and have required us to raise substantial amounts of additional capital during this period. We expect to continue to incur operating losses for the foreseeable future as we secure customers for and continue to invest in the commercialization of our IC products. Due to the strong commitment of our resources to research and development and expansion of our product offerings to customers, we will need to increase revenues substantially beyond levels that we have attained in the past in order to generate sustainable operating profit and sufficient cash flows to continue doing business without raising additional capital from time to time. Given our history of fluctuating revenues and operating losses, the expected reduction in royalty and licensing revenues and challenges we face in securing customers for our IC products, we cannot be certain that we will be able to achieve profitability on either a quarterly or annual basis in the future. The possibility that we will not be able to meet our obligations as and when they become due over the next twelve months raises substantial doubt about our ability to continue as a going concern.

Accordingly, we have been pursuing, and will continue to pursue, the implementation of certain cost reduction strategies. Additionally, we are seeking additional financing and evaluating financing alternatives in order to meet our cash requirements for the next 12 months. We may not be able to obtain additional financing, as needed, on acceptable terms, or at all, which may require us to further reduce our operating costs and other expenditures, including additional reductions of personnel and capital expenditures. Alternatively, or in addition to such potential measures, we may elect to implement other cost reduction actions as we may determine are necessary and in our best interests, including the possible sale or cessation of certain of our business segments. Any such actions undertaken might limit our opportunities to realize plans for revenue growth, and we might not be able to reduce our costs in amounts sufficient to achieve break-even or profitable operations. If we issue additional equity or convertible debt securities to raise funds, the ownership percentage of our existing stockholders would be reduced and they may experience significant dilution. New investors may demand rights, preferences or privileges senior to those of existing holders of our common stock. If we are not successful in these actions, we may be forced to cease operations. See Management’s Discussion and Analysis of Financial Condition, “Results of Operations, Liquidity and Capital Resources, and Going

Concern-Working Capital."

Our auditor has expressed substantial doubt about our ability to continue as a going concern and, absent additional financing, we may be unable to remain a going concern.

In light of our recurring losses, accumulated deficit and negative cash flow, as described in the notes to our consolidated financial statements, the report of our independent registered public accounting firm on our financial statements for the year ended December 31, 2016 contains an explanatory paragraph raising substantial doubt about our ability to continue as a going concern. Our consolidated financial statements do not include any adjustments that may be necessary in the event we are unable to continue as a going concern. If we do not raise enough additional capital sufficient

Table of Contents

to allow for the removal of this going concern uncertainty, we will need to significantly modify our operational plans for us to continue as a going concern.

Our failure to raise additional capital or generate the significant capital necessary to expand our operations and invest in the new products could reduce our ability to compete and could harm our business.

We intend to continue spending substantial amounts to grow our business. In March 2016, we issued $8 million aggregate principal amount of 10% Subordinate Senior Secured Convertible Notes due August 15, 2018 (the Notes). The Note principal is convertible into our common stock, as well as the interest on the Notes, as we have the option of paying the interest in-kind by converting such interest into additional note principal. In addition, the Notes also include limited anti-dilution protection, such that the conversion price will be reset to a lower conversion price in some situations. As a result, our stockholders may experience significant dilution of these Notes and any additional paid-in-kind principal are converted into our common stock and the conversion price is reset. We will still need to obtain additional financing to pursue our business strategy, develop new products, respond to competition and market opportunities and acquire complementary businesses or technologies. There can be no assurance that such additional capital, whether in the form of debt or equity financing, will be sufficient or available and, if available, that such capital will be offered on terms and conditions acceptable to us. We are exploring various alternatives, and expect to implement cost reductions to successfully sustain the business. If we are unsuccessful in these efforts, we will need to implement significant cost reduction strategies that could affect our near- and long-term business plan. These efforts may include, but are not limited to reducing headcount and curtailing business activities, especially around new product development.

If we were to raise additional capital through sales of our equity securities, our stockholders would suffer dilution of their equity ownership. If we engage in a subsequent debt financing, we may be required to accept terms that restrict our ability to incur additional indebtedness, prohibit us from paying dividends, repurchasing our stock or making investments, and force us to maintain specified liquidity or other ratios, any of which could harm our business, operating results and financial condition. If we need additional capital and cannot raise it on acceptable terms, we may not be able to, among other things:

- Develop or enhance our products;
- Continue to expand our product development and sales and marketing organizations;
- Acquire complementary technologies, products or businesses;
- Expand operations, in the United States or internationally;
- Hire, train and retain employees; or
- Respond to competitive pressures or unanticipated working capital requirements.

Our failure to do any of these things could seriously harm our ability to execute our business strategy and may force us to curtail our research and development plans or existing operations.

We currently lack the funds to repay the convertible notes due in August 2018.

In March 2016, we entered into a 10% Senior Secured Convertible Note Purchase Agreement with the purchasers of the Notes. Accrued interest is payable semi-annually in cash or in kind through the issuance of identical new Notes, or with a combination of the two, at our option. Through August 2017, we have made the interest payments in-kind through the issuance of additional notes totaling approximately $1.2 million. The notes are secured by substantially all of our assets. If we fail to pay the Notes, including accrued interest, in full when due, the holders of the Notes, acting through their agent, will be entitled to pursue all of their remedies as secured creditors, including taking possession of the collateral securing the Notes and effecting a private sale of some or all of our assets securing the Notes. After the holders of the

Table of Contents

Notes take such actions, we may not have enough assets to make payments owed to other creditors, to continue operating our business, or distribute any funds to stockholders.

Our success depends upon the networking and communications systems markets' acceptance of our ICs.

The future prospects of our business depend on the adoption and acceptance by our target markets, networking communications and data center equipment providers, of our Bandwidth Engine and LineSpeed ICs. In 2011, we began focusing our engineering, marketing and sales efforts on our IC products and de-emphasizing our technology licensing activities, which historically have been our primary revenue source. Our prospective customers may be unwilling to adopt and design-in our ICs due to the uncertainties and risks surrounding designing a new IC into their systems and relying on a supplier that has almost no history of manufacturing such ICs. In addition, our Bandwidth Engine IC products require our customers and their other IC suppliers to implement our new and proprietary chip-to-chip communication protocol, GCI, which they may be unwilling to do. We have determined and negotiated prices with a few customers for our ICs and have gained only limited experience with the cost of making and selling these products. Thus, currently, we do not know whether we will be able to profitably make and sell these products. We are investing significant resources to develop our next generation IC products, but may not introduce these new products successfully or obtain significant revenue from them.

An important part of our strategy to gain market acceptance is to penetrate new markets by targeting market leaders to accept our IC solutions. This strategy is designed to encourage other participants in those markets to follow these leaders in adopting our solutions. If a high-profile industry participant adopts our ICs for one or more of its products but fails to achieve success with those products, or is unable to successfully implement our ICs, other industry participants' perception of our solutions could be harmed. Any such event could reduce the amount of future sales of our IC products.

Our future revenue depends on our winning designs with our customers, and those customers designing our solutions into their product offerings and successfully selling and marketing such products. If we do not continue to win designs in the short term, our product revenue in the following years will not grow.

We sell our ICs to original equipment manufacturer (OEM) customers that include our ICs in their products. Our technology is generally incorporated into products at the design stage, which we refer to as a design win, and which we define as the point at which a customer has made a commitment to build a board against a fixed schematic for his system, and this board will utilize our ICs. As a result, our future revenue depends on our OEM customers designing our ICs into their products, and on those products being produced in volume and successfully commercialized. If we fail to convince our current or prospective customers to include our ICs in their products and fail to achieve a consistent number of design wins, our results of operations and business will be harmed. In addition, if a current or prospective customer designs a competitor's offering into its product, it becomes significantly more difficult for us to sell our IC solutions to that customer because changing suppliers involves significant cost, time, effort and risk for the OEM. Even if a customer designs one of our ICs into its product, we cannot be assured that the OEM's product will be commercially successful over time or at all or that we will receive or continue to receive any revenue from that customer. Furthermore, the customer product for which we obtain a design win may be canceled before the product enters production or is introduced into the market. Because of our extended sales cycle, our revenue in future years is highly dependent on design wins we are awarded today. Our lack of capital and uncertainty about our future technology roadmap also may limit our success in achieving additional design wins, as discussed under, "Our auditor has expressed substantial doubt about our ability to continue as a going concern, and, absent additional financing, we may be unable to remain a going concern," and "We may experience difficulties in transitioning to new wafer fabrication process technologies or in achieving higher levels of design integration, which may result in reduced manufacturing yields, delays in product deliveries and increased costs."

The design win process is generally a lengthy, expensive and competitive process, with no guarantee of revenue, and if we fail to generate sufficient revenue to offset our expenses, our business and operating results would suffer.

Achieving a design win is typically a lengthy, expensive and competitive process because our customers generally take a considerable amount of time to evaluate our ICs. In the markets we serve, the time from initial customer engagement to design win to production volume shipments can range from two to three years, though it may take longer for new customers or markets we intend to address. In order to win designs, we are required to both incur design and development

Table of Contents

costs and dedicate substantial engineering resources in pursuit of a single customer opportunity. Even though we incur these costs, we may not prevail in the competitive selection process and, even if we do achieve a design win, we may never generate sufficient, or any, revenue to offset our development expenditures. Our customers have the option to decide whether or not to put our solutions into production after initially designing our products in the specification. The customer can make changes to its product after a design win has been awarded to us, which can have the effect of canceling a previous design win. The delays inherent in our protracted sales cycle increase the risk that a customer will decide to cancel, curtail, reduce or delay its product plans, causing us to lose anticipated revenue. In addition, any change, delay or cancellation of a customer's plans could harm our financial results, as we may have incurred significant expense while generating no revenue.

If our foundries do not achieve satisfactory yields or quality, our cost of goods sold will increase, our operating margins will decline, and our reputation and customer relationships could be harmed.

We depend not only on sufficient foundry manufacturing capacity and wafer prices, but also on good production yields (the number of good die per wafer) and timely wafer delivery to meet customer demand and maintain profit margins. The fabrication of our products is a complex and technically demanding process. Minor deviations in the manufacturing process can cause substantial decreases in yields, and in some cases, cause production to be suspended. Our foundry, Taiwan Semiconductor Manufacturing Company (TSMC), from time to time, experiences manufacturing defects and reduced manufacturing yields. Changes in manufacturing processes or the inadvertent use of defective or contaminated materials by our foundries could result in lower than anticipated manufacturing yields, which would harm our revenue or increase our costs. For example, recently, our foundry produced ICs and met its process specification range but did not meet our customer's specifications causing us to write off a portion of our production lot. Many of these problems are difficult to detect at an early stage of the manufacturing process and may be time consuming and expensive to correct. Poor yields from our foundry, or defects, integration issues or other performance problems in our ICs, could cause us significant customer relations and business reputation problems, harm our operating results and give rise to financial or other damages to our customers. Our customers might consequently seek damages from us for their losses. A product liability claim brought against us, even if unsuccessful, would likely be time consuming and costly to defend.

We may experience difficulties in transitioning to new wafer fabrication process technologies or in achieving higher levels of design integration, which may result in reduced manufacturing yields, delays in product deliveries and increased costs.

We aim to use the most advanced manufacturing process technology appropriate for our solutions that is available from TSMC. As a result, we periodically evaluate the benefits of migrating our solutions to other technologies in order to improve performance and reduce costs. These ongoing efforts require us from time to time to modify the manufacturing processes for our products and to redesign some products, which in turn may result in delays in product deliveries. We are dependent on TSMC to support the production of wafers for future versions of our ICs, as TSMC is our sole foundry. Such production may require changes to TSMC's existing process technology. If TSMC elects to not alter their process technology to support future versions of our ICs, we would need to identify a new foundry.

In addition, specifically with regard to our Bandwidth Engine products, our 1T-SRAM technology is not available at process nodes below 40 nanometers. To date, we have not developed any memory products below the 40 nanometer process node. To continue the product roadmap for our Bandwidth Engine and PSE products, we will need to identify a new foundry and/or no longer use our 1T-SRAM technology. We do not consider this to adversely affect our current product offerings, but we expect to face difficulties, delays and increased expense as we transition our products to new processes, and potentially to new foundries for future products. For example, we believe our next generation of products will need to be designed using a FinFET process, which will require us to incur significantly high development costs for mask tooling and computer-aided design software. We currently lack the funds to pay for such

development costs. Moreover, an inability to continue our product roadmap can adversely affect, and has in the past affected our efforts to win new customers, secure additional design wins and significantly grow our future revenues.

Because the manufacturing of integrated circuits is extremely complex, the process of qualifying a new foundry is a lengthy process and there can be no assurance that we will be able to find and qualify replacement suppliers without materially adversely affecting our business, financial condition, results of operations and prospects for future growth. We

Table of Contents

cannot assure you that we will be able to maintain our relationship with our foundries or develop relationships with new foundries. If we or TSMC experience significant delays in transitioning to smaller geometries or fail to efficiently implement transitions, we could experience reduced manufacturing yields, delays in product deliveries and increased costs, any of which could harm our relationships with our customers and our operating results.

We may not achieve the anticipated benefits of becoming a fabless semiconductor company by developing and bringing to market the Bandwidth Engine and LineSpeed IC product lines.

In 2010, we expanded our business model to become a fabless semiconductor company through the development of a product line of memory ICs called the Bandwidth Engine. In March 2013, we announced a product line of SerDes ICs called LineSpeed. Our goal is to increase our total available market by creating high-performance ICs for networking communications and data center systems, using our proprietary technology and design expertise. This development effort has required that we add headcount and design resources, such as expensive software tools, which has increased our losses from and cash used in operations. We may not be successful in our development efforts to bring our ICs to market successfully nor be successful in selling ICs due to various risks and uncertainties, including, but not limited to:

- Our lack of working capital;
- customer acceptance;
- adoption of the GCI protocol, without which our Bandwidth Engine products cannot function;
- difficulties and delays in our product development, manufacturing, testing and marketing activities;
- timeliness of new product introductions;
- the anticipated costs and technological risks of developing and bringing ICs to market;
- the willingness of our manufacturing partners to assist successfully with fabrication;
- our ability to qualify our products for mass production and achieve wafer yield levels and the final test results necessary to be price competitive;
- the availability of quantities of ICs supplied by our manufacturing partners at a competitive cost;
- our ability to generate the desired gross margin percentages and return on our product development investment;
- competition from established IC suppliers;
- the adequacy of our intellectual property protection for our proprietary IC designs and technologies;
- customer concerns over our financial condition and viability to be a long-term profitable supplier;
- the vigor and growth of markets served by our current and prospective customers; and
- our lack of recent experience as a fabless semiconductor company making and selling proprietary ICs.

If we experience significant delays in bringing our IC products to market or if customer adoption of our products is delayed, this could have a material adverse effect on our anticipated revenues in upcoming years due to the potential loss of design wins and future revenues. For example, we have experienced significant delays in bringing our third generation LineSpeed products to market, which has prevented us from achieving design wins and resulted in us introducing products after our competitors. We may continue to experience significant delays in the future.

Table of Contents

Our main objective is the development and sale of our products to networking communications and data center systems providers and their subsystem and component vendors, and, if demand for these products does not grow, we may not achieve revenue growth and our strategic objectives.

We market and sell our ICs to networking communications and data center equipment providers and their subsystem and component vendors. We believe our future business and financial success depends on market acceptance and increasing sales of these products. In order to meet our growth and strategic objectives, networking infrastructure OEMs must incorporate our products into their systems, and the demand for their systems must grow as well. We cannot provide assurance that sales of our products to these OEMs will increase substantially in the future or that the demand for our customers' systems will increase. Our future revenues from these products may not increase in accordance with our growth and strategic objectives if instead our OEM customers modify their product designs, select products sold by our competitors or develop their own proprietary ICs. Moreover, demand for their products that incorporate our ICs may not grow or result in significant sales of such products due to factors affecting the customers and their business, such as industry downturns, declines in capital spending in the enterprise and carrier markets and unfavorable macroeconomic conditions. Thus, the future success of our business depends in large part on factors outside our control, and sales of our products may not meet our revenue growth and strategic objectives.

Our failure to continue to develop new products and enhance our products on a timely basis could diminish our ability to attract and retain customers.

The existing and potential markets for our products are characterized by ever-increasing performance requirements, evolving industry standards, rapid technological change and product obsolescence. These characteristics lead to frequent new product introductions and enhancements, shorter product life cycles and changes in industry demands. In order to attain and maintain a significant position in the market, we will need to continue to enhance and evolve our products and the underlying proprietary technologies in anticipation of these market trends.

Our future performance depends on a number of factors, including our ability to:

- identify target markets and relevant emerging technological trends;
- develop and maintain competitive technology by improving performance and adding innovative features that differentiate our products from alternative technologies;
- enable the incorporation of our products into the customers' products on a timely basis and at competitive prices;
- develop our products to be manufactured at smaller process geometries; and
- respond effectively to new technological developments or new product introductions by others.

Our failure to develop future products that achieve market acceptance could harm our competitive position and impede our future growth.

Our ICs have a lengthy sales cycle, which makes it difficult to predict success in this market and the timing of future revenue.

Our ICs have a lengthy sales cycle, ranging from six to 24 months from the date of our initial proposal to a prospective customer until the date on which the customer confirms that it has designed our product into its system. As lengthy, or an even lengthier period, could ensue before we would know the volume of products that such customer will, or is likely to, order. A number of factors can contribute to the length of the sales cycle, including technical evaluations of our products by the customers, the design process required to integrate our products into the customers' products and the timing of the customers' new product announcements. In anticipation of product orders, we may incur substantial costs before the sales cycle is complete and before we receive any customer payments. As a result, in the event that a sale is not

11

Table of Contents

completed or is cancelled or delayed, we may have incurred substantial expenses, making it more difficult for us to become profitable or otherwise negatively impacting our financial results. Furthermore, because of this lengthy sales cycle, the recording of revenues from our selling efforts may be substantially delayed, our ability to forecast our future revenue may be more limited and our revenue may fluctuate significantly from quarter to quarter. We cannot provide any assurances that our efforts to build a strong and profitable business based on the sale of ICs will succeed. If these efforts are not successful, in light of the substantial resources that we have invested, our future operating results and cash flows could be materially and adversely affected.

The semiconductor industry is cyclical in nature and subject to periodic downturns, which can negatively affect our revenue.

The semiconductor industry is cyclical and has experienced pronounced downturns for sustained periods of up to several years. To respond to any downturn, many semiconductor manufacturers and their customers will slow their research and development activities, cancel or delay new product developments, reduce their workforces and inventories and take a cautious approach to acquiring new equipment and technologies. As a result, our business has been in the past and could be adversely affected in the future by an industry downturn, which could negatively impact our future revenue and profitability. Also, the cyclical nature of the semiconductor industry may cause our operating results to fluctuate significantly from year-to-year, which may tend to increase the volatility of the price of our common stock.

We expect our licensing and royalty revenues to decrease compared with our historical results, and there is no guarantee revenues from our IC products will replace these lost revenues in the near future.

In 2011, we began to place greater emphasis on our IC business and re-deploy engineering, marketing and sales resources from IP to IC activities. We are no longer actively pursuing new license arrangements, and, as a result, our license and royalty revenues in 2016 declined when compared with prior years. We do not expect to generate sufficient revenues from our IC business to allow us to achieve profitability in 2017. In addition, the production volumes of the current royalty-bearing products shipped by our licensees are expected to decrease; therefore we expect our royalty revenue to decrease in 2017 and future periods. Historically, royalties have generated a 100% gross margin, and any decrease in royalties adversely affects our gross margin, operating results and cash flows.

Our revenue has been highly concentrated among a small number of licensees and customers, and our results of operations could be harmed if we lose a key revenue source and fail to replace it.

Our overall revenue has been highly concentrated, with a few customers accounting for a significant percentage of our total revenue. For the year ended December 31, 2016, our three largest customers represented 47%, 21% and 13% of total revenue, respectively. For the year ended December 31, 2015, our three largest customers represented 34%, 31% and 12% of total revenue, respectively. For the year ended December 31, 2014, our three largest customers represented 34%, 31% and 11% of total revenue, respectively. We expect that a relatively small number of customers will continue to account for a substantial portion of our revenue for the foreseeable future.

As a result of this revenue concentration, our results of operations could be adversely affected by the decision of a single key licensee or customer to cease using our technology or products or by a decline in the number of products that incorporate our technology that are sold by a single licensee or customer or by a small group of licensees or customers.

Our revenue concentration may also pose credit risks, which could negatively affect our cash flow and financial condition.

We might also face credit risks associated with the concentration of our revenue among a small number of licensees and customers. As of December 31, 2016, four customers represented 88% of total trade receivables. Our failure to collect receivables from any customer that represents a large percentage of receivables on a timely basis, or at all, could adversely affect our cash flow or results of operations and might cause our stock price to fall.

Table of Contents

Our products must meet exact specifications, and defects and failures may occur, which may cause customers to return or stop buying our products.

Our customers generally establish demanding specifications for quality, performance and reliability that our products must meet. However, our products are highly complex and may contain defects and failures when they are first introduced or as new versions are released. If defects and failures occur in our products during the design phase or after, we could experience lost revenues, increased costs, including warranty and customer support expenses and penalties for non-performance stipulated in customer purchase agreements, delays in or cancellations or rescheduling of orders or shipments, product returns or discounts, diversion of management resources or damage to our reputation and brand equity, and in some cases consequential damages, any of which would harm our operating results. In addition, delays in our ability to fill product orders as a result of quality control issues may negatively impact our relationship with our customers. We cannot assure you that we will have sufficient resources to satisfy any asserted claims. Furthermore, any such defects, failures or delays may be particularly damaging to us as we attempt to establish our reputation as a reliable provider of IC products.

Because we sell our products on a purchase order basis and rely on estimated forecasts of our customers' needs, inaccurate forecasts could adversely affect our business.

We expect to sell our IC products pursuant to individual purchase orders, rather than long-term purchase commitments. Therefore, we will rely on estimated demand forecasts, based upon input from our customers, to determine how much product to manufacture. Because our sales will be based primarily on purchase orders, our customers may cancel, delay or otherwise modify their purchase commitments with little or no notice to us. For these reasons, we will generally have limited visibility regarding our customers' product needs. In addition, the product design cycle for networking OEMs is lengthy, and it may be difficult for us to accurately anticipate when they will commence commercial shipments of products that include our ICs.

Furthermore, if we experience substantial warranty claims, our customers may cancel existing orders or cease to place future orders. Any cancellation, delay or other modification in our customers' orders could significantly reduce our revenue, cause our operating results to fluctuate from period to period and make it more difficult for us to predict our revenue. In the event of a cancellation or reduction of an order, we may not have enough time to reduce operating expenses to mitigate the effect of the lost revenue on our business.

If we overestimate customer demand for our products, we may purchase products from our manufacturers that we cannot sell. Conversely, if we underestimate customer demand or if sufficient manufacturing and testing capacity were unavailable, we would forego revenue opportunities and could lose market share in the markets served by our products and could incur penalty payments under our customer purchase agreements. In addition, our inability to meet customer requirements for our products could lead to delays in product shipments, force customers to identify alternative sources and otherwise adversely affect our ongoing relationships with our customers.

We depend on contract manufacturers for a significant portion of our revenue from the sale of our IC products.

Many of our current and prospective OEM customers use third party contract manufacturers to manufacture their systems, and these contract manufacturers purchase our products directly from us on behalf of the OEMs. Although we expect to work with our OEM customers in the design and development phases of their systems, these OEMs often give contract manufacturers some authority in product purchasing decisions. If we cannot compete effectively for the business of these contract manufacturers, or, if any of the contract manufacturers that work with our OEM customers experience financial or other difficulties in their businesses, our revenue and our business could be adversely affected. For example, if a contract manufacturer becomes subject to bankruptcy proceedings, we may not be able to obtain our products held by the contract manufacturer or recover payments owed to us by the contract manufacturer for products

already delivered to the contract manufacturer. If we are unable to persuade contract manufacturers to purchase our products, or if the contract manufacturers are unable to deliver systems with our products to OEMs on a timely basis, our business would be adversely affected.

Table of Contents

We rely on independent foundries and contractors for the manufacture, assembly, testing and packaging of our integrated circuits, and the failure of any of these third parties to deliver products or otherwise perform as requested could damage our relationships with our customers and harm our sales and financial results.

As a fabless semiconductor company, we rely on third parties for substantially all of our manufacturing operations. We depend on these parties to supply us with material in a timely manner that meets our standards for yield, cost and quality. We do not have long-term supply contracts with any of our suppliers or manufacturing service providers, and therefore they are not obligated to manufacture products for us for any specific period, in any specific quantity or at any specified price, except as may be provided in a particular purchase order. Any problems with our manufacturing supply chain could adversely impact our ability to ship our products to our customers on time and in the quantity required, which in turn could damage our customer relationships and impede market acceptance of our IC solutions.

Our third party wafer foundries, testing and assembly vendors and sales offices are located in regions at high risk for earthquakes and other natural disasters. Any disruption to the operations of these foundries, vendors and offices resulting from earthquakes or other natural disasters could cause significant delays in the development, production, shipment and sales of our IC products.

TSMC, which manufactures our products, is located in Asia, as are other foundries we may use in the future. EAG, which handles the testing of our products, is headquartered in California. Our primary engineering design center is located in Santa Clara, California, and we have sales offices in Japan and China. The risk of an earthquake in the Pacific Rim region is significant due to the proximity of major earthquake fault lines. In September 1999, a major earthquake in Taiwan affected the facilities of several major foundries and other vendors. As a result of this earthquake, these vendors suffered power outages and disruptions that impaired their production capacity. In September 2003 and February 2016, additional disruptive earthquakes occurred in Taiwan. The occurrence of additional earthquakes or other natural disasters could result in the disruption of the wafer foundry or assembly and test capacity of the third parties that supply these services to us and may impede our research and development efforts, as well as our ability to market and sell our products. We may not be able to obtain alternate capacity on favorable terms, if at all.

Any claim that our products or technology infringe third party intellectual property rights could increase our costs of operation and distract management and could result in expensive settlement costs or the discontinuance of our technology licensing or product offerings. In addition, we may incur substantial litigation expense, which would adversely affect our profitability.

The semiconductor industry is characterized by vigorous protection and pursuit of intellectual property rights or positions, which has resulted in often protracted and expensive litigation. We are not aware of any third party intellectual property that our products or technology would infringe. However, like many companies of our size with limited resources, we have not searched for all potentially applicable intellectual property in the public databases. It is possible that a third party now has, or may in the future obtain, patents or other intellectual property rights that our products or technology may now, or in the future, infringe. Our licensees and IC customers, or we, might, from time to time, receive notice of claims that we have infringed patents or other intellectual property rights of others. Litigation against us can result in significant expense and divert the efforts of our technical and management personnel, whether or not the litigation has merit or results in a determination adverse to us.

Royalty amounts owed to us might be difficult to verify, and we might find it difficult, expensive and time-consuming to enforce our license agreements.

The standard terms of our 1T-SRAM license agreements require our licensees to document the manufacture and sale of products that incorporate our technology and generally report this data to us after the end of each quarter. We have

the right to audit these royalty reports periodically, although we have not conducted any such audits since 2010. These audits can be expensive, time-consuming and potentially detrimental to our business relationships. A failure to fully enforce the royalty provisions of our license agreements could cause our revenue to decrease and impede our ability to achieve and maintain profitability.

Table of Contents

We might not be able to protect and enforce our intellectual property rights, which could impair our ability to compete and reduce the value of our technology.

Our technology is complex and is intended for use in complex SoCs and networking systems. Our licensees' products utilize our embedded memory and/or I/O technology, and a large number of companies manufacture and market these products. Because of these factors, policing the unauthorized use of our intellectual property is difficult and expensive. We cannot be certain that we will be able to detect unauthorized use of our technology or prevent other parties from designing and marketing unauthorized products based on our technology. In the event we identify any past or present infringement of our patents, copyrights or trademarks, or any violation of our trade secrets, confidentiality procedures or licensing agreements, we cannot assure you that the steps taken by us to protect our proprietary information will be adequate to prevent misappropriation of our technology. Our inability to adequately protect our intellectual property would reduce significantly the barriers of entry for directly competing technologies and could reduce the value of our technology. Furthermore, we might initiate claims or litigation against third parties for infringement of our proprietary rights or to establish the validity of our proprietary rights. Litigation by us could result in significant expense and divert the efforts of our technical and management personnel, whether or not such litigation results in a determination favorable to us.

Our existing patents might not provide us with sufficient protection of our intellectual property, and our patent applications might not result in the issuance of patents, either of which could reduce the value of our core technology and harm our business.

We rely on a combination of patents, trademarks, copyrights, trade secret laws and confidentiality procedures to protect our intellectual property rights. As of December 31, 2017, we held 69 patents in the United States, and approximately 38 foreign patents, which expire at various times from 2018 to 2035. In addition, as of December 31, 2017, we also held 10 pending patent applications worldwide. We cannot be sure that any patents will be issued from any of our pending applications or that any claims allowed from pending applications will be of sufficient scope or strength, or issued in all countries where our products can be sold, to provide meaningful protection or any commercial advantage to us. In December 2011, we sold 43 United States and 30 related foreign patents, which reduced the size of our patent portfolio and diminishes our ability to assert counterclaims in the defense of actions against us that may arise. Also, competitors might be able to design around our patents. Failure of our patents or patent applications to provide meaningful protection might allow others to utilize our technology without any compensation to us.

The discovery of defects in our technology and products could expose us to liability for damages.

The discovery of a defect in our technologies and products could lead our customers to seek damages from us. Many of our agreements with customers include provisions waiving implied warranties regarding our technology and products and limiting our liability to our customers. We cannot be certain, however, that the waivers or limitations of liability contained in our agreements with customers will be enforceable.

If we fail to retain key personnel, our business and growth could be negatively affected.

Our business has been dependent to a significant degree upon the services of a small number of executive officers and technical employees. The loss of key personnel could negatively impact our technology development efforts, our ability to deliver under our existing agreements, maintain strategic relationships with our partners, and obtain new customers. We generally have not entered into employment or non-competition agreements with any of our employees and do not maintain key-man life insurance on the lives of any of our key personnel.

We may incur additional debt in the future, subject to certain limitations contained in our senior secured convertible notes.

The degree to which we are leveraged and the restrictions governing our indebtedness could have important consequences including, but not limited to:

· limiting our ability to service all of our debt obligations;

Table of Contents

- impacting our ability to incur additional indebtedness or obtain additional financing in the future for working capital, capital expenditures, acquisitions or general corporate or other purposes;
- increasing our vulnerability to general economic downturns and adverse industry conditions;
- limiting our flexibility in planning for, or reacting to, changes in our business and our industry; and
- limiting our ability to engage in certain transactions or capitalize on acquisition or other business opportunities.

If we are in violation of the terms of the Notes in the future and do not receive a waiver, the note holders could choose to accelerate payment on all outstanding loan balances. If we needed to obtain replacement financing, we may not be able to quickly obtain equivalent or suitable replacement financing. If we are unable to secure alternative sources of funding, such acceleration would have a material adverse impact on our financial condition.

Our failure to successfully address the potential difficulties associated with our international operations could increase our costs of operation and negatively impact our revenue.

We are subject to many difficulties posed by doing business internationally, including:

- foreign currency exchange fluctuations;
- unanticipated changes in local regulation;
- potentially adverse tax consequences, such as withholding taxes and transfer pricing issues;
- political and economic instability; and
- reduced or limited protection of our intellectual property.

Because we anticipate that integrated circuit sales to companies that operate primarily outside the United States may account for a substantial portion of our revenue in future periods, the occurrence of any of these circumstances could significantly increase our costs of operation, delay the timing of our revenue and harm our profitability.

Provisions of our certificate of incorporation and bylaws or Delaware law might delay or prevent a change of control transaction and depress the market price of our stock.

Various provisions of our certificate of incorporation and bylaws might have the effect of making it more difficult for a third party to acquire, or discouraging a third party from attempting to acquire, control of our company. These provisions could limit the price that certain investors might be willing to pay in the future for shares of our common stock. Certain of these provisions eliminate cumulative voting in the election of directors, limit the right of stockholders to call special meetings and establish specific procedures for director nominations by stockholders and the submission of other proposals for consideration at stockholder meetings.

We are also subject to provisions of Delaware law which could delay or make more difficult a merger, tender offer or proxy contest involving our company. In particular, Section 203 of the Delaware General Corporation Law prohibits a Delaware corporation from engaging in any business combination with any interested stockholder for a period of three years unless specific conditions are met. Any of these provisions could have the effect of delaying, deferring or preventing a change in control, including without limitation, discouraging a proxy contest or making more difficult the acquisition of a substantial block of our common stock.

Under our certificate of incorporation, our board of directors may issue up to 20,000,000 shares of preferred stock without stockholder approval on such terms as the board might determine. The rights of the holders of common stock will

Table of Contents

be subject to, and might be adversely affected by, the rights of the holders of any preferred stock that might be issued in the future.

Our stockholder rights plan could prevent stockholders from receiving a premium over the market price for their shares from a potential acquirer.

We adopted a stockholder rights plan that generally entitles our stockholders to rights to acquire additional shares of our common stock when a third party acquires 15% of our common stock or commences or announces its intent to commence a tender offer for at least 15% of our common stock, other than for one group of related stockholders, as to whom this threshold is 20%. The plan also includes an exception to permit the acquisition of shares representing more than 15% of our common stock by a brokerage firm that manages independent customer accounts and generally does not have any discretionary voting power with respect to such shares. This plan could delay, deter or prevent an investor from acquiring us in a transaction that could otherwise result in stockholders receiving a premium over the market price for their shares of common stock. Our intention is to maintain and enforce the terms of this plan, which could delay, deter or prevent an investor from acquiring us in a transaction that could otherwise result in stockholders receiving a premium over the market price for their shares of common stock.

Potential volatility of the price of our common stock could negatively affect your investment.

We cannot assure you that there will continue to be an active trading market for our common stock. Historically, the stock market, as well as our common stock, has experienced significant price and volume fluctuations. Market prices of securities of technology companies have been highly volatile and frequently reach levels that bear no relationship to the operating performance of such companies. These market prices generally are not sustainable and are subject to wide variations. If our common stock trades to unsustainably high levels, it is likely that the market price of our common stock will thereafter experience a material decline. In the past, our board of directors approved stock repurchase programs, and any future program could impact the price of our common stock and increase volatility.

In the past, securities class action litigation has often been brought against a company following periods of volatility in the market price of its securities. We could be the target of similar litigation in the future. Securities litigation could cause us to incur substantial costs, divert management’s attention and resources, harm our reputation in the industry and the securities markets and negatively impact our operating results.

Our stock price could drop, and there could be significantly less trading activity in our stock, if securities or industry analysts downgrade our stock or do not publish research or reports about our business.

Our stock price and the trading market for our stock are likely to be affected significantly by the research and reports concerning our company and our business which are published by industry and securities analysts. We do not have any influence or control over these analysts, their reports or their recommendations. Our stock price and the trading market for our stock could be negatively affected if any analyst downgrades our stock, publishes a report which is critical of our business, or discontinues coverage of us.

Table of Contents

We are a “smaller reporting company” and, as a result of the reduced disclosure and governance requirements applicable to smaller reporting companies, our common stock may be less attractive to investors.

We are a “smaller reporting company,” meaning that we are not an investment company, an asset-backed issuer, or a majority-owned subsidiary of a parent company that is not a “smaller reporting company,” have a public float of less than $75 million and have annual revenues of less than $50 million during the most recently completed fiscal year. As a “smaller reporting company,” we are subject to lesser disclosure obligations in our SEC filings compared to other issuers. Specifically, “smaller reporting companies” are able to provide simplified executive compensation disclosures in their filings, are exempt from the provisions of Section 404(b) of the Sarbanes-Oxley Act requiring that independent registered public accounting firms provide an attestation report on the effectiveness of internal control over financial reporting and have certain other decreased disclosure obligations in their SEC filings, including, among other things, only being required to provide two years of audited financial statements in annual reports. Decreased disclosures in our SEC filings due to our status a “smaller reporting company” may make it harder for investors to analyze our operating results and financial prospects.

If we fail to maintain compliance with the continued listing requirements of the Nasdaq Capital Market, our common stock may be delisted and the price of our common stock and our ability to access the capital markets could be negatively impacted.

Our common stock currently trades on The NASDAQ Stock Market (Nasdaq) under the symbol “MOSY.” This market has continued listing standards that we must comply with in order to maintain the listing of our common stock. The continued listing standards include, among others, a minimum bid price requirement of $1.00 per share and any of: (i) a minimum stockholders’ equity of $2.5 million; (ii) a market value of listed securities of at least $35.0 million; or (iii) net income from continuing operations of $500,000 in the most recently completed fiscal year or in the two of the last three fiscal years. Our results of operations and fluctuating stock price directly impact our ability to satisfy these continued listing standards. In the event we are unable to maintain these continued listing standards, our common stock may be subject to delisting from the Nasdaq Capital Market.

On July 14, 2016, we received a deficiency letter from the Listing Qualifications Department (the Staff) of Nasdaq providing notification that the Company was not in compliance with Nasdaq’s audit committee composition requirements pursuant to Nasdaq Listing Rule 5605(c)(2). Nasdaq Listing Rule 5605 requires a listed company to have an audit committee comprised of at least three independent members and, during 2016, the number of independent directors on our Audit Committee was reduced from three to two. The letter also stated that we would be provided: (i) until the earlier of our next annual shareholders’ meeting or June 24, 2017. On October 6, 2017, we received a letter from Nasdaq notifying us that we had regained compliance with Nasdaq’s audit committee, independent director and compensation committee requirements for continued listing. The letter noted that with the appointments of Daniel Lewis and Daniel O’Neil to our board of directors on September 26, 2017, we had regained compliance with Nasdaq Marketplace Rules 5605(c)(2), 5605(b)(1) and 5605(d)(2). On October 18, 2017, we received a deficiency letter from the Listing Qualifications Department (of The NASDAQ Stock Market ("Nasdaq") providing notification that, for the previous 30 consecutive business days, the bid price for the Company's common stock had closed below the minimum $1.00 per share requirement for continued inclusion on the Nasdaq Global Select Market pursuant to Nasdaq Listing Rule 5450(a)(1). On November 30, 2017, Nasdaq informed us that, as of November 28, 2017, we evidenced a closing bid price of our common stock in excess of the $1.00 minimum requirement for the last 10 consecutive trading days, and that, accordingly, we had regained compliance with Nasdaq Marketplace Rule 5550(a)(2) and NASDAQ considered the matter closed.

We have received similar deficiency letters from time to time prior to 2017, and may receive them again in the future. Ultimately such deficiencies, if not remedied, could cause Nasdaq to delist our common stock. If we are delisted, we would expect our common stock to be traded in the over-the-counter market, which could adversely affect the

liquidity of our common stock. Additionally, we could face significant material adverse consequences, including:

- a limited availability of market quotations for our common stock;
- a reduced amount of analyst coverage;

Table of Contents

- a decreased ability to issue additional securities or obtain additional financing in the future;
- reduced liquidity for our stockholders;
- potential loss of confidence by customers, collaboration partners and employees; and
- loss of institutional investor interest.

USE OF PROCEEDS

All shares of our common stock offered by this prospectus are being registered for the account of the selling stockholders. We will not receive any of the proceeds from the sale of these shares. We will receive proceeds from the cash exercise of the warrants which, if exercised in cash with respect to all of the 662,500 shares of common stock, would result in gross proceeds of $1,556,875 to us before commissions and expenses. We intend to use the net proceeds, if any, received from the exercise of the warrants for working capital and other general corporate purposes.

MARKET INFORMATION FOR OUR COMMON STOCK

The following table sets forth the range of high and low sales prices of our common stock on the NASDAQ Capital Market for the periods indicated:

	High	Low
2017		
First Quarter (January 1 – March 31, 2017)	$ 4.32	$ 2.00
Second Quarter (April 1 – June 30, 2017)	$ 2.70	$ 0.64
Third Quarter (July 1 – September 30, 2017)	$ 1.81	$ 0.89
Fourth Quarter (October 1 – December 31, 2017)	$ 1.45	$ 0.64

Dividend Policy

We have never declared or paid any cash dividends on our common stock and do not currently anticipate declaring or paying cash dividends on our common stock in the foreseeable future. We currently intend to retain all of our future earnings, if any, to finance operations. Any future determination relating to our dividend policy will be made at the discretion of our board of directors and will depend on a number of factors, including future earnings, capital requirements, financial conditions, future prospects, contractual restrictions and other factors that our board of directors may deem relevant.

Holders of Record

As of December 31, 2017, there were 6 holders of record of our common stock. The actual number of stockholders is greater than this number of record stockholders and includes stockholders who are beneficial owners but whose shares are held in street name by brokers and other nominees. This number of stockholders of record also does not include stockholders whose shares may be held in trust by other entities.

Stock Performance Graph

The following graph compares cumulative total stockholder return on our common stock with that of the S&P 500 Index and the S&P Technology Sector Index from 2012 through 2017. The comparison assumes that $100 was invested on December 31, 2012 in our common stock, the stocks included in the S&P 500 Index and the stocks

included in the S&P Technology Sector Index. We have never paid any cash dividends to holders of our common stock.

The comparisons shown in the graph below are based upon historical data, and we caution that the stock price performance shown in the graph below is not indicative of, nor intended to forecast, the potential future performance of our common stock. Information used in the graph was obtained from Standard and Poor's website, a source believed to be reliable, but we are not responsible for any errors or omissions in such information.

Table of Contents

Comparison of Five-Year Cumulative Return

	12/31/2012	12/31/2013	12/31/2014	12/31/2015	12/31/2016	12/31/2017
MOSYS, INC.	$ 100.00	$ 158.62	$ 53.74	$ 31.32	$ 6.61	$ 3.19
S & P 500	100.00	129.60	144.36	143.31	156.98	187.47
S & P TECHNOLOGY SECTOR	100.00	127.97	154.19	158.92	177.96	243.65

Securities Authorized for Issuance under Equity Compensation Plan

The following table provides information as of December 31, 2017 regarding equity compensation plans approved by our security holders. As of December 31, 2017, we had no awards outstanding under equity compensation plans that have not been approved by our security holders.

Plan Category	Number of Securities to be Issued Upon Exercise of Outstanding Options, Warrants and Rights (a)	Weighted Average Exercise Price of Outstanding Options, Warrants and Rights (b)	Number of Securities Remaining Available for Future Issuance under Equity Compensation Plans (excluding Securities reflected in Column (a))(1) (c)
Equity compensation plans approved by security holders	683,934	$ 4.81	378,209

(1) Consists of shares of common stock available for future issuance under the Equity Plan and shares of common stock available for future issuance under the Amended and Restated 2010 Employee Stock Purchase Plan. The Equity Plan provides for an annual increase of 50,000 shares on January 1 of each year.

BUSINESS

Overview

We are a fabless semiconductor company focused on the development and sale of integrated circuits, or ICs, for the high-speed networking, communications, storage and computing markets. Our solutions deliver time-to-market, performance, signal integrity, power, area and economic benefits for system original equipment manufacturers, or OEMs. We have developed two IC product lines under the Bandwidth Engine and LineSpeed product names. Bandwidth Engine ICs integrate our proprietary 1T-SRAM high-density embedded memory with our integrated macro function technology and a highly efficient serial interface protocol resulting in a monolithic memory IC solution optimized for transaction performance. As the bandwidth requirements and amount of processing per packet increase in high-speed networking systems, critical memory access bottlenecks occur. Our Bandwidth Engine IC, with its combination of serial I/O, high-speed memory, offload functions and efficient, intelligent access, drastically increases memory accesses per second, removing these bottlenecks. In addition, the serial interface and high memory capacity

reduce the board footprint,

Table of Contents

number of pins and complexity while using less power. The LineSpeed IC product line, which we announced in March 2013, is comprised of non-memory, high-speed serialization-deserialization, or SerDes, I/O physical layer, or PHY, devices that ensure signal integrity between interfaces which is commonly referred to as clock data recovery, or CDR, or retimer functionality, which perform multiplexing to transition from one speed to another, commonly referred to as Gearbox functionality. These PHY devices reside within optical modules and networking equipment line cards designed for next-generation Ethernet and optical transport network applications.

We are currently supporting existing design win customers, primarily for Bandwidth Engine, and actively pursuing additional design wins for the use of our ICs in networking, communications and data center equipment. We have established initial pricing of our IC products ordered to date, but longer-term volume prices will be subject to negotiations with our customers and may vary substantially from these initial prices.

Prior to 2010, our primary business was the design, development, marketing, sale and support of differentiated intellectual property, or IP, including embedded memory and high-speed parallel and serial I/O used in advanced systems-on-chips, or SoCs. Currently, we are focused on developing differentiated IP-rich IC products and are dedicating all our research and development, marketing and sales budgets to these IC products. Royalty and other revenue generated from our existing IP agreements represented 45% of our total revenue in 2015 and 24% in 2016. We expect royalty and other revenue to continue to decline in 2018 both in absolute dollars and as a percentage of revenues.

Our future success and ability to achieve and maintain profitability are dependent on the marketing and sales of our IC products into networking, communications and other markets. Since the beginning of 2010, we have invested substantially all of our of our research and development resources toward development of our ICs, and, as of the end of 2012, had ceased our efforts to actively market our IP and establish license agreements for customers' new SoC development projects.

Industry Background

The amount of data being transferred by networking, storage and computing systems is increasing rapidly, primarily driven by the growth of the Internet and demand for real-time processing of bandwidth intensive applications, such as video-on-demand, Internet protocol TV, peer-to-peer and cloud computing, web 2.0 applications, 4G/LTE wireless, voice-over-Internet protocol, and many others. In order to meet these demands, the network backbone, access, storage and data center infrastructure must scale in bandwidth and processing capability. In addition, system designers face the challenge of increasing the throughput of all subsystems for a variety of applications, such as video games, medical record and imaging transfers, and file sharing. These increased demands strain communication between onboard IC devices, limiting the data throughput in network switches and routers and the network backbone.

To meet these demands, carrier and enterprise networks are undergoing significant changes and, most significantly, are migrating to packet-based Ethernet networks that enable higher throughput, lower cost and uniform technology across access, core and metro network infrastructure. These networks are now being designed to deliver voice, video and high-speed Internet access on one converged, efficient and flexible network. These trends require networking systems, especially the high-speed switches and routers that primarily comprise these networks, to comply with evolving market requirements and be capable of providing new services and better quality of service while supporting new protocols and standards. To support these trends, OEM network and telecommunications equipment manufacturers, such as Alcatel-Lucent (a subsidiary of Nokia Corporation), Brocade Communications Systems, Inc., Cisco Systems, Inc., Tel. LM Ericsson, Fujitsu Ltd., Hitachi Ltd., Huawei Technologies, Juniper Networks, Inc., Nokia Corporation, and ZTE Corporation, must offer higher levels of packet forwarding rates, bandwidth density and be optimized to enable higher-density, lower power data path connectivity in the next generations of their networking systems.

Networking and telecommunications systems throughout the network must operate at higher speed and performance levels and so require new generations of packet processors and improved memory subsystems, as well as new physical interface products, to enable system performance. These systems and their component line cards generally need to support aggregate rates of 100 gigabits per second, or Gbps, and above to meet the continued growth in network traffic. Cloud services have accelerated this transition with applications such as security. Data centers and access equipment that were previously aggregating slower traffic such at 1Gbps to 10Gbps, and 40Gbps, now are being designed

Table of Contents

to aggregate traffic at 10Gbps to 100Gbps, or more. The transition to 100 Gbps networks has begun, and 100 Gbps networks are expected to grow rapidly over the coming years.

Several types of semiconductors are included on each line card, including PHY, one or more packet processors and multiple memory chips. Packet processors are complex ICs or IC chipsets that perform high speed processing for functions, such as traffic routing, shaping, metering, billing, statistics, detection and steering. The line cards use various types of memory ICs to facilitate temporary packet storage and assist in the analysis and tracking of information embedded within each packet flowing through the processors. After a packet enters the line card through a PHY, a packet or data processor helps separate the packet into smaller pieces for rapid analysis. Typically, the data is broken up into the packet header, which contains vital information on packet destination and type, such as the Internet protocol address, and the payload, which contains the data being sent. Generally, the line card operations must occur at full data rates and typically require accessing memory ICs many times. Simultaneously, the packet's payload, which may be substantially larger than the packet header, is also stored in memory ICs until processing is complete and the packet can re-combine and be sent to its next system destination. Within the line card, communication between the packet processor and memory ICs occurs through an interface consisting of combinations of physical pins on each type of chip. These pins are grouped together in a parallel or a serial architecture to form a pathway, called a bus, through which information is transferred from one IC to the next.

Today, the majority of physical buses that connect networking equipment and components use a parallel architecture to communicate between processors and memory ICs, which means information can travel only in one direction and in one instance at a time. As processing speeds increase, the number of pins required and the speed of the bus in a parallel architecture become a limitation on system performance and capability. In contrast, the number of connections is reduced substantially across fewer, higher-rate pins in a serial architecture, and data is transferred simultaneously in both directions. Data transfer rates with high-speed serial bus architectures and more advanced I/O protocols are limited by the capabilities of the various ICs included on the line card, thus leading to bottlenecks when these ICs perform inadequately. In order to remove these bottlenecks and meet next-generation bandwidth requirements, the line card ICs must support high-speed serial bus architectures and these more advanced I/O protocols.

Most networking and communication systems sold and in operation today include line cards that process data at speeds ranging from 10 Gbps, to 100 Gbps, and support many aggregated slower ports. To accommodate the substantial and growing increase in demand for networking communications and applications, networking systems manufacturers are developing and bringing to market next-generation systems that run at aggregate speeds of 100 to 400 Gbps or more with developments underway to scale to thousands of Gbps, or terabits, per second. However, although processor performance in applications such as computing and networking has continued to double nearly every 18 months, or even sooner, the performance of memory technology has generally been able to double only once every 10 years. Existing memory IC solutions based on parallel I/O architecture easily support speeds up to 40 Gbps, but are not optimal for meeting speeds of 100 Gbps and beyond due to system-level limitations for pin counts, power and performance. These networking and communications systems are generally comprised of a chassis populated by four to 16 line cards. Often, these systems are shipped to customers with only a portion of the line card slots populated, and the customer will add additional line cards subsequently to increase system performance and capacity.

Each line card requires a significant amount of memory to support its processing capabilities. Traditional external memory IC solutions currently used on line cards include both dynamic random access memory, or DRAM, and static random access memory, or SRAM. Line cards in networking systems use both specialized, high-performance DRAM ICs, such as reduced-latency DRAM, or RLDRAM, low-latency DRAM, or LLDRAM, and commodity DRAM, such as double data rate, or DDR ICs. In addition, networking systems use higher-performance SRAM ICs such as quad data rate, or QDR SRAM. Substantially all of these traditional memory IC solutions use parallel interfaces, which are slower than serial interfaces, so we believe they will be increasingly challenged to meet the performance, pin count, area and power requirements as networking systems expand beyond 100 Gbps. The result is a gap between processor

and memory performance. To meet the higher performance requirements being demanded by the industry, while using current components and architectural approaches, system designers must add more discrete memory ICs to the line cards and/or add more embedded memory on the packet processor. This results in higher cost and power consumption, the use of more space on the line cards and additional communication interference between the ICs, which in turn results in additional

Table of Contents

bandwidth limitation problems. We believe our Bandwidth Engine family of products is well suited to address these challenges and replace these traditional memory solutions.

In addition, each line card requires PHY products to provide interoperability and signal integrity functions. As network speeds increase beyond 100Gbps, the serial data rates are transitioning from 10Gbps to 25Gbps. This means that the signal integrity challenges (maintaining the quality of the electrical signals) of moving these high speed signals around within line cards, or between line cards and systems using fiber optic or copper cable, increase as data rates increase. These networking systems often use copper or optical modules to modify signals for transmission over longer distances ranging from tens of meters to thousands of kilometers. Optical modules convert electrical signals to optical signals for transportation over longer distances from one system to another system. Because of the challenges arising from the increase in network speeds, new 100Gbps standards have emerged that specify a CDR or retimed interface on optical modules, which was not the case at 10Gbps based interfaces. Each 100Gbps module and above using 25Gbps per lane will require a CDR/retimer function inside the module to meet these requirements. In addition, the systems themselves also require additional support to move signals between the module and the system, and these challenges become more acute as the distance increases. Our LineSpeed products address these new line card and optical module challenges by providing unique signal integrity and feature sets that align with the industry standards, as well as provide backward compatibility for the previous data rates. We believe our LineSpeed PHY products are well suited ensure the quality of signals and/or increase the transmission distance for both short reach (e.g., between ICs on a line card) or long-reach (e.g., between line cards or systems).

We have developed our Bandwidth Engine and LineSpeed families of ICs to synergistically address the need for high-speed data access and throughput currently confronting networking system designers. We expect our IC products to meet the increasing demands placed on conventional memory technology used on the line cards in high-bandwidth networking systems. We believe that our products and technology are well positioned as replacements for existing IC solutions in order to meet the needs of the next-generation networking systems that will require a large number of packet lookups and to support aggregated rates greater than 100 Gbps.

Our Approach

Our historical business was focused on the licensing of our proprietary 1T- SRAM and SerDes I/O technologies. We have leveraged our proprietary IP to design our Bandwidth Engine and LineSpeed IC product families to help networking OEMs address the growing bottlenecks in system performance. We have incorporated critical features into our product families to accomplish this objective.

On-Chip Functionality

One significant performance bottleneck in any network line card is the need to transfer data between discrete ICs. Many of these data-transfer operations are iterative in nature, requiring subsequent, back-to-back accesses of the memory IC by the processor IC. Our Bandwidth Engine ICs include an arithmetic logic unit, or ALU, which enables the Bandwidth Engine IC to perform mathematical operations on data. Moving certain processing functions from the processor IC to the Bandwidth Engine IC through the use of this embedded ALU, reduces the number of I/O transactions and frees the processor IC to perform other important networking or micro-processing functions.

High-Performance Interface

High-speed, efficient interface I/Os are critical building blocks to meet high data transfer rate requirements for communication between ICs on network line cards. We believe that current networking system requirements necessitate an industry transition from parallel to serial I/O. As a result, semiconductor companies are increasingly turning to serial I/O architectures to achieve needed system performance. For example, high-performance ICs that are

sold into wide markets, such as field programmable gate arrays, or FPGAs, and network processing units, NPUs, are using serial I/Os to ensure they can compete with custom designed application specific ICs, or ASICs, by matching their performance. Using serial I/O, IC developers also are able to reduce pin count (the wired electrical pins that connect an IC to the network line card on which it is mounted) on the IC. With reducing geometries, the size of most high-performance ICs is dictated by the number of pins required, rather than the amount of logic and memory embedded in the chip. As a result, using serial

Table of Contents

I/O facilitates cost reduction and reduced system power consumption, while improving the performance of both the IC itself and the overall system. While SerDes I/Os provide significantly enhanced performance over parallel I/Os, SerDes I/Os traditionally have had higher power consumption, which is a challenge for IC designers. Our SerDes I/Os, however, are tuned for low power consumption to meet our customers' stringent power consumption requirements.

We make our I/O technologies compliant with industry standards so that they can interoperate with interfaces on existing ICs. In addition, we make them programmable to support multiple data rates, which allows for greater flexibility for the system designer, while lowering their development and validation costs. Interoperability reduces development time, thereby reducing the overall time to market of our customers' systems.

Analog Design Capabilities

We have invested in personnel needed to define, design and market high- performance analog IC products. We have built a team of experienced engineers who combine industry expertise with advanced semiconductor design expertise to meet customer requirements and develop new products to bring to market. We initially developed our team of analog engineers to develop the SerDes I/O used in our Bandwidth Engine families of products. We leveraged the capabilities of this team to produce our LineSpeed IC products, which are primarily comprised of analog circuitry.

GigaChip Interface Protocol

In addition to the physical characteristics of the serial I/O, the protocol used to transmit data is also an important element that impacts speed and performance. To address this and complement our Bandwidth Engine devices, we have developed the GigaChip Interface®, or GCI, which is an open-interface transport protocol optimized for efficient chip-to-chip communications. The GCI electrical interface is compatible with the current industry standard (Common Electrical Interface, release #11, or CEI-11G-SR and XFI) to simplify electrical interoperability between devices. GCI can enable highly efficient serial chip-to-chip communications, and its transport efficiency averages 90% for the data transfers it handles. GCI is included in our Bandwidth Engine ICs, and is offered to customers and prospective partners on terms intended to encourage widespread adoption.

High-Performance and High-Density Memory Architecture

The high-density of our proprietary 1T-SRAM technologies stems from the use of a single-transistor, or 1T, which is similar to DRAM, with a storage cell for each bit of information. Embedded memory utilizing our 1T-SRAM technologies is typically two to three times denser than the six-transistor storage cells used by traditional SRAM, or 6T-SRAM. Embedded memory utilizing our 1T-SRAM technologies typically provides speeds essentially equal to or greater than the speeds of traditional SRAM and DRAM, particularly for larger memory sizes. Our 1T-SRAM memory designs can sustain random access cycle times of less than three nanoseconds, significantly faster than embedded 6T-SRAM technology. Embedded memory utilizing our 1T-SRAM technologies can consume as little as one-half the active power and generate less heat than traditional SRAM when operating at the same speed. This reduces system level heat dissipation and enables reliable operation using lower cost packaging.

Our Strategy

Our primary business objective is to be an IP-rich fabless semiconductor company offering ICs that deliver unparalleled memory bandwidth performance for packet processing and improved signal integrity performance for networking, security and data center systems. The key components of the expansion of our strategic plan to become an IC supplier include the following strategies:

Target Large and Growing Markets

Our initial strategy is to target the multi-billion dollar networking telecommunications, security and data center OEM equipment markets, and we have developed products to support the growth in 100 Gbps and higher networking speeds. We are currently supporting approximately 25 existing customers, with whom we have achieved over 85 design wins, which reflects broadening acceptance of our products. We define a design win as the point at which a customer has

Table of Contents

made a commitment to build a board against the fixed schematic for his system, and this board will utilize our IC products. We continue to actively pursue additional design wins for the use of our ICs in our target markets. We believe our design wins represent the potential for significant future revenues. With limited history to date, however, we cannot estimate how much revenue each design win is likely to generate, or how much revenue all of these (and future design wins) are likely to generate. For example, our first design wins from 2012 and 2013 are starting to ramp into production, and, while we cannot predict how steep these ramps might be, we expect our revenues from them to grow in successive periods over the next few years. However, there is no assurance that these customer designs will be shipped in large volume by our customers to their customers.

Leverage Technologies to Create New Products

Our strategy is to combine our proprietary IP and design and applications expertise to address the needs of several upcoming generations of advanced networking systems. We believe an IC combining our 1T-SRAM and serial I/O with logic, such as in an ALU, and other functions can provide a system-level solution and significantly improve overall system performance at lower cost while using less power. We also seek to leverage our high-speed serial I/O to create non-memory denominated ICs, such as our LineSpeed products. Our initial LineSpeed products targeted the line card and the same customers as our Bandwidth Engine products. This has given us the opportunity to provide both memory and PHY solutions during the sale process. In 2013, we introduced our first LineSpeed products to address the requirements new industry standards were placing on optical modules, as well as line cards.

Expand Adoption of the GigaChip Interface Protocol

We have provided our GCI interface protocol as an open industry standard that may be designed into other ICs in the system, as we believe this will further enable serial communication on network line cards and encourage adoption of our Bandwidth Engine IC products. A number of IC providers and partners have publicly announced their support of GCI and Bandwidth Engine, including the largest FPGA providers, Altera Corporation (a subsidiary of Intel Corporation), Xilinx, Inc., and EZchip Semiconductor Ltd. (a subsidiary of Mellanox Technologies Ltd.), with whom we work closely to support common customers. In addition, multiple networking systems companies, including actual and prospective customers, have adopted GCI.

Build Long-Term Relationships with Suppliers of Packet Processors

We believe that having long-term relationships with packet processor providers is critical to our success, as such relationships may enable us to reduce our time-to-market, provide us with a competitive advantage and expand our target markets. A key consideration of network system designers is to demonstrate interoperability between our Bandwidth Engine IC and the packet processors utilized in their systems. To obtain design wins for our Bandwidth Engine IC, we must demonstrate this interoperability, and also show that our IC works optimally with the packet processor to achieve the performance requirements. In addition, our current strategy requires packet processor suppliers to adopt our GCI interface. To that end, we have been working closely with FPGA, ASIC and NPU providers, to enable interoperability between our Bandwidth Engine IC products and their high-performance products. To facilitate the acceptance of our Bandwidth Engine ICs, we have made available development and characterization kits for system designers to evaluate and develop code for next-generation networking systems. Our characterization kits are fully-functional hardware platforms that allow FPGA and ASIC providers, and their customers, to demonstrate interoperability of the Bandwidth Engine IC with the ASIC or FPGA the designers use within their networking systems. Our recent announcement of the third-generation Bandwidth Engine Z30 device, designed for interoperability with the EZ-chip NPS-400, is an example and direct result of this strategy.

Our Products

Bandwidth Engine

The Bandwidth Engine is a memory-dominated IC that has been designed to be a high-performance companion IC to packet processors. While the Bandwidth Engine primarily functions as a memory device with a high-performance and high-efficiency interface, it also can accelerate certain processing operations by serving as a co-processor element. Our Bandwidth Engine ICs combine: (1) our proprietary high-density, high-speed, low latency embedded memory, (2) our

Table of Contents

high-speed serial interface technology, or SerDes, (3) an open-standard interface protocol and (4) intelligent access technology. We believe an IC combining our 1T-SRAM memory and serial I/O with logic and other intelligence functions provides a system-level solution and significantly improves overall system performance at lower cost, size and power consumption. Our Bandwidth Engine ICs can provide up to and over 4.5 billion memory accesses per second, which is more than twice the performance of current memory-based solutions. They also can enable system designers to significantly narrow the gap between processor and memory IC performance. Customers that design Bandwidth Engine ICs onto the line cards in their networking systems will re-architect their systems at the line-card level and use our product to replace traditional memory solutions. When compared with existing commercially available solutions, our Bandwidth Engine ICs may:

- provide up to four times the performance;
- reduce power by approximately 50%;
- reduce cost by greater than 50%; and
- result in a dramatic reduction in IC pin counts on the line card.

Our first generation Bandwidth Engine IC products contain 576 megabytes, or MB, of memory and use a serial I/O with up to 16 lanes operating at up to 10.3 Gbps per lane. Variations of this IC can have up to two interface ports, with up to eight serial receiver and eight serial transmitter lanes per port for a total of 16 lanes of 10.3 Gbps SerDes interface. These ICs include an ALU, which can perform read-modify-write operations. We have been shipping our initial Bandwidth Engine products since 2012. We have notified customers, however, that we intend to discontinue our BE1 products. We expect to complete final shipments of our BE1 products by the end of 2018.

Our second generation Bandwidth Engine IC products contain 576 MB of memory and use serial I/O with up to 16 lanes operating at up to 15 Gbps per lane. In addition to a speed improvement of up to 50%, the architecture will enable several family member parts with added specialized features. To date, we have announced three unique devices in this product family:

- MSR620 with burst features optimized for oversubscription buffer applications;
- MSR720 with a write cache and memory coherency capability that allows for deterministic look-ups optimized for state and queue type applications; and
- MSR820 with increased intelligence for lookup, metering and statistics applications by adding dual counters, atomic and extensive metering functions.

We have been shipping our Bandwidth Engine 2 IC products since 2013.

Our third generation Bandwidth Engine IC products contain 1152 MB of memory and use serial I/O with up to 16 lanes operating at up to 30 Gbps per lane. Bandwidth Engine 3 targets support for packet-processing applications with up to five billion memory single word accesses per second, as well as burst mode to enable full duplex buffering up to 400Gbps for ingress, egress and oversubscription applications. To date, we have announced three unique devices in this product family:

- MSR630 enables high rate lookup or high-performance buffer capabilities;
- MSR830 offers additional offload capabilities for functions such as statistics and metering to increase performance and add features for next-generation networking and communications equipment; and

Table of Contents

- MSRZ30 builds upon the capabilities and performance of the MSR830, with data rates, interface protocol and data structures that are optimized for the EZchip NPS-400 network processing unit, or NPU, and can increase memory bandwidth by up to 50%.

We commenced sampling of these products in the first quarter of 2016.

The devices provide benefits of size, power, pin count and cost savings to our customers. We do not anticipate significant revenues from these products until 2018 or later.

Programmable Search Engine

We brought our Programmable Search Engine, or PSE, IC products to market in early 2016 to further leverage our proven serial interface technology and high-density integrated memory with the processor engine architecture to enable high-speed customizable search, security, and data analysis functions for networking, security, and data center applications. Our PSE architecture features 32 search-optimized processor engines, data flow schedulers, and over a terabit of internal access bandwidth. The device leverages our GCI technology and high-density integrated memory (1152 Mb of 1T-SRAM® embedded memory). The PSE device's 32 processor elements have direct access to integrated table memory through an internal interconnect and scheduler architecture.

LineSpeed

Our first generation LineSpeed products consist of single-chip PHY ICs, including a 100G multi-mode gearbox and a 100G quad retimer. These devices are designed to support 10, 40 and 100Gbps standards for high-density line cards or modules for next generation ethernet and optical transport network applications. These devices are capable of supporting both short and long reach connections across different specifications. We have developed these PHY ICs to provide the CDR function and to provide signal conversion from lower rates to higher rates both on the line card and within the optical module. We have defined performance and form factor (sizes) for specific devices for optimization of features and performance to solve space challenges both on the line card and in the optical module. We introduced and began sampling these devices in 2013.

Our second generation of LineSpeed products consists of our 100G low power retimer, which is optimized for ultra low power consumption, integrated test features and small size. The low-power retimer is primarily targeting opportunities in 100G CFP2, CFP4 and QSFP28 optical modules and active copper cables. We introduced and began sampling this product in 2014.

Our third generation of LineSpeed products, the Flex family of 100G PHYs, is designed to support the latest industry standards and includes gearbox, Multi-Link Gearbox, or MLG, and high density CDR/retimer devices designed to enable existing and next generation Ethernet and OTN line card applications to support the latest high-density electrical and optical interfaces. To date, we have announced four unique devices in this product family:

- MSH320, a 100Gbps Gearbox with RS-FEC: For adapting 10x10 to 4x25 from 100Gbps optical standards to a host ASIC, MAC/Framer, NPU or FPGA with 10x10G interfaces. The MSH320 includes an integrated Reed-Solomon forward error correction, or RS-FEC, option to enable systems to also support new electrical and optical standards. The device also includes a 10x10Gbps retimer to allow seamless support of 10 and 40Gbps interfaces;
- MSH225, a 10 Lane Full-Duplex Retimer: For high-density retiming applications where the line rates may be up to 28Gbps per lane and connect to host ASIC, framer, NPU or FPGA ICs equipped with 25Gbps interfaces. Each one of the 20 total independent lanes can be configured to support 10, 25, 40 or 100Gbps standards. The MSH225 integrates optional 100Gbps RS-FEC capability and includes a unique redundant link mode feature to support redundancy, scaling or monitoring features;
.

MSH322, a 100Gbps Multi-Link Gearbox for Line Cards for support of high-density, independent 10GE and 40GE interfaces multiplexed into a 100GE (4x25Gbps) host interface, while supporting the latest optical

Table of Contents

industry standards. The device enables line cards with high-density switches based on 25Gbps interfaces to support two times the density of 10 and 40Gbps ports; and

- MSH321, a derivative Multi-Link Gearbox built into a highly compact package and optimized layout to support the MLG function in module and compact daughter card applications.

While we have a robust pipeline of design win opportunities, to date, less than 10% of our design wins claimed are for our LineSpeed products, and we have notified these customers that we do not intend to support these products going forward.

IP Licensing and Distribution

Historically, we have offered our memory and I/O technologies on a worldwide basis to semiconductor companies, electronic product manufacturers, foundries, intellectual property companies and design companies through product development, technology licensing and joint marketing relationships. We licensed our IP technology to semiconductor companies who incorporated our technology into ICs that they sold to their customers. As a result of the change in our corporate strategy, since early 2012, our IP licensing activities have been limited, and we expect this to continue. However, for the nine months ended September 30, 2017, 7% of our total revenues were generated from royalties related to our existing licensing arrangements, as we continue to collect royalties from 1T-SRAM licensees. Licensing and royalty revenues have been declining since 2010, and we expect continued decline in 2018.

Research and Development

Our ability to compete in the future depends on successfully improving our technology to meet the market's increasing demand for higher performance and lower cost requirements. We have assembled a team of highly skilled engineers whose activities are focused on developing higher density, higher bandwidth, higher speed and lower cost next generation IC products. Development of our IC products requires specialized chip design and product engineers, as well as significant fabrication and testing costs, including mask costs, as we bring these products to market. We expect our significant future research and development activities to include:

- designing next generation ICs with larger memory blocks and higher-speed SerDes;
- developing versions of our Bandwidth Engine ICs with alternative features, such as lower-speed SerDes, increased chip-level intelligence or smaller memory blocks to allow us to serve a broader range of applications and system requirements;
- developing derivative versions of our LineSpeed ICs to meet customer demands; and
- developing new products that can leverage our proprietary IP portfolio and expand our market opportunity.

No development efforts are being dedicated to creating new or enhanced technology solely for use in licensing offerings.

Sales and Marketing

We believe that networking and communications systems OEMs typically prefer to extend the use of traditional memory solutions and their parallel interfaces, despite performance and costs challenges and are reluctant to change their technology platforms and adopt new designs and technologies, such as serial interfaces, which are an integral part of our product solutions. Therefore, our principal selling and marketing activities to date have been focused on persuading these OEMs and key component specialists that our solutions provide critical performance advantages, as well as on securing design wins with them.

Table of Contents

Our sales and marketing personnel are located in the United States, Japan and China. In addition to our direct sales team, we sell through sales representatives and distributors in the United States and Asia. We also have multiple applications engineers who support our customer engagements and work closely with our engineering team on product definition. For our products, our applications engineers must engage with the customers' system architects and designers to propose our IC and IP solutions such as the GCI Interface, to address their systems challenges.

In the markets we serve, the time from initial customer engagement to design win to production volume shipments can range from 18-36 months. Networking and communications systems can have a product life from a few years to over 10 years once a product like ours has been designed into the system.

Our revenue has been highly concentrated, with a few customers accounting for a significant percentage of our total revenue. For the year ended December 31, 2016, Alcatel-Lucent, Kogent, Inc., our Japanese IC distributor and Taiwan Semiconductor Manufacturing Co., Ltd., or TSMC, represented 47%, 21% and 13% of total revenue, respectively. For the year ended December 31, 2015, Alcatel-Lucent, TSMC and Kogent, Inc. represented 34%, 31% and 12% of total revenue, respectively. For the year ended December 31, 2014, TSMC, Kogent, Inc. and Broadcom Ltd. represented 34%, 31% and 11% of total revenue, respectively.

Customers in North America accounted for 63%, 51% and 28% of our revenues for the years ended December 31, 2016, 2015 and 2014, respectively. Customers in Japan accounted for 22%, 15% and 36% of our revenues for the years ended December 31, 2016, 2015 and 2014, respectively. Customers in Taiwan accounted for 13%, 32% and 35% of our revenues for the years ended December 31, 2016, 2015 and 2014, respectively. Our remaining revenues were primarily from customers in the rest of Asia and in Europe.

Intellectual Property

We regard our patents, copyrights, trademarks, trade secrets and similar intellectual property as critical to our success, and rely on a combination of patent, trademark, copyright, and trade secret laws to protect our proprietary rights.

As of December 31, 2017, we held 69 U.S. and 38 foreign patents on various aspects of our technology, with expiration dates ranging from 2018 to 2035. We also held 10 pending patent applications in the U.S. and abroad. There can be no assurance that others will not independently develop or patent similar or competing technology or design around any patents that may be issued to us, or that we will be able to successfully enforce our patents against infringement by others.

In December 2011, we sold 43 United States and 30 related foreign memory technology patents for $35 million in cash pursuant to a patent purchase agreement. Under the agreement, we retained a license to all of the sold patents that is unlimited with respect to our development, manufacturing and distribution of our Bandwidth Engine IC product line and any other proprietary products that we develop as long as they are not DRAM ICs. We also retained the rights necessary to renew existing 1T-SRAM licenses and to grant licenses similar in scope to identified foundries. We also retained rights to grant licenses for our second source purposes, to enable certain kinds of technology development and, to a limited extent, for certain ASIC products that incorporate one of our technology macros. However, the patent purchase agreement limits our rights to grant licenses under the sold patents outside the scope of our retained license and, in particular, limits the number of future licenses of 1T-SRAM memory technology that we can grant to developers of SoCs, which used to be the principal focus of our 1T-SRAM licensing activities.

The semiconductor industry is characterized by frequent litigation regarding patent and other intellectual property rights. Our licensees or we might, from time to time, receive notice of claims that we have infringed patents or other intellectual property rights owned by others. Our successful protection of our patents and other intellectual property rights and our ability to make, use, import, offer to sell, and sell products free from the intellectual property rights of

others are subject to a number of factors, particularly those described in Part I, Item 1A, “Risk Factors.”

Table of Contents

Competition

The markets for our products are highly competitive. We believe that the principal competitive factors are:

- processing speed and performance;
- density and cost;
- power consumption;
- reliability;
- interface requirements;
- ease with which technology can be customized for and incorporated into customers' products; and
- level of technical support provided.

We believe that our products compete favorably with respect to each of these criteria. Our proprietary 1T-SRAM embedded memory and high-speed serial I/O IP can provide our Bandwidth Engine ICs with a competitive advantage over alternative devices. Alternative solutions are either DRAM or SRAM-based and can support either the memory size or speed requirements of high-performance networking systems, but generally not both. DRAM solutions provide a significant amount of memory at competitive cost, but DRAM solutions do not have the required fast access and cycle times to enable high-performance. The DRAM solutions currently used in networking systems include RLDRAM from Micron Technology, Inc., or Micron, and Integrated Silicon Solutions, Inc., LLDRAM from Renesas and DDR from Samsung Electronics Co., Ltd., Micron and others. In addition, Micron has a hybrid memory cube DRAM product, which consists of multiple DRAMs connected with a serial interface. SRAM solutions can meet high-speed performance requirements, but often lack adequate memory size. The SRAM solutions currently used in networking systems primarily include QDR or similar SRAM products from Cypress Semiconductor Corporation and GSI Technology, Inc. The majority of the currently available SRAM and DRAM solutions use a parallel, rather than a serial I/O. To offset these drawbacks, system designers generally must use more discrete memory ICs, resulting in higher power consumption and greater utilization of space on the line card.

Our competitors include established semiconductor companies with significantly longer operating histories, greater name recognition and reputation, large customer bases, dedicated manufacturing facilities and greater financial, technical, sales and marketing resources. This may allow them to respond more quickly than us to new or emerging technologies or changes in customer requirements. Many of our competitors also have significant influence in the semiconductor industry. They may be able to introduce new technologies or devote greater resources to the development, marketing and sales of their products than we can. Furthermore, in the event of a manufacturing capacity shortage, these competitors may be able to manufacture products when we are unable to do so.

Our Bandwidth Engine ICs compete with embedded memory solutions, stand-alone memory ICs, including both DRAM and SRAM ICs, and ASICs designed by customers in-house to meet their system requirements. Our prospective customers may be unwilling to adopt and design-in our ICs due to the uncertainties and risks surrounding designing a new IC into their systems and relying on a supplier that has limited history of manufacturing such ICs. In addition, Bandwidth Engine ICs require the customer and its other IC suppliers to implement our chip-to-chip communication protocol, the GCI interface. These parties may be unwilling to do this if they believe it could adversely impact their own future product developments or competitive advantages, or, if they believe it might complicate their development process or increase the cost of their products. In order to remain competitive, we believe we must provide unparalleled memory IC solutions with the highest bandwidth capability for our target markets, which solutions are engineered and built for high-reliability carrier and enterprise applications.

Table of Contents

Manufacturing

We depend on third-party vendors to manufacture, package, assemble and test our IC products, as we do not own or operate a semiconductor fabrication, packaging or production testing facility for boards and system assembly. By outsourcing manufacturing, we are able to avoid the high cost associated with owning and operating our own facilities, allowing us to focus our efforts on the design and marketing of our products.

We perform an ongoing review of product manufacturing and testing processes. Our IC products are subjected to extensive testing to assess whether their performance meets design specifications. Our test vendors provide us with immediate test data and the ability to generate characterization reports that are made available to our customers. We have achieved ISO 9001:2008 certification, and all of our manufacturing vendors have also achieved ISO 9001 certification.

Employees

As of December 31, 2017, we had 24 employees located in the United States, consisting of 10 in research and development and manufacturing operations and 14 in sales, general and administrative.

Available Information

We were founded in 1991 and reincorporated in Delaware in September 2000. Our website address is www.mosys.com. The information in our website is not incorporated by reference into this report. Through a link on the Investor section of our website, we make available our annual reports on Form 10-K, quarterly reports on Form 10-Q, current reports on Form 8-K, and any amendments to those reports filed or furnished pursuant to Section 13(a) or 15(d) of the Securities Exchange Act of 1934, as soon as reasonably practicable after they are filed with, or furnished to, the Securities and Exchange Commission, or SEC. You can also read and obtain copies of any materials we file with the SEC at the SEC's Public Reference Room at 450 Fifth Street, NW, Washington, DC 20549. You can obtain additional information about the operation of the Public Reference Room by calling the SEC at 1.800.SEC.0330. In addition, the SEC maintains a website (www.sec.gov) that contains reports, proxy and information statements, and other information regarding issuers that file electronically with the SEC, including us.

Properties

Our principal administrative, sales, marketing, operations and research and development functions are located in a leased facility in San Jose, California. We currently occupy approximately 10,000 square feet of space in the San Jose facility, the lease for which extends through November 2020. We believe that our existing facilities are adequate to meet our current needs.

Legal Proceedings

We are not a party to any material legal proceeding which could have a material adverse effect on our consolidated financial position or results of operations. From time to time, we may be subject to legal proceedings and claims in the ordinary course of business. These claims, even if not meritorious, could result in the expenditure of significant financial resources and diversion of management efforts.

MANAGEMENT'S DISCUSSION AND ANALYSIS OF FINANCIAL CONDITION AND RESULTS OF OPERATIONS

This Management's Discussion and Analysis of Financial Condition and Results of Operations should be read in conjunction with the accompanying consolidated financial statements and notes included in this prospectus.

Overview

Our strategy and primary business objective is to become a fabless semiconductor company focused on the development and sale of integrated circuits, or ICs, for the high-speed networking, communications, storage and data

Table of Contents

center markets. Our solutions deliver time-to-market, performance, power, area and economic benefits for system original equipment manufacturers, or OEMs. We have developed two families of ICs under the Bandwidth Engine® and LineSpeed™ product names. Bandwidth Engine ICs combine our proprietary 1T-SRAM® high-density embedded memory, integrated macro functions and high-speed serial interface, or SerDes, I/O, with our intelligent access technology and a highly efficient interface protocol. The LineSpeed IC product line, which was announced in March 2013, is comprised of non-memory, high-speed SerDes I/O devices with clock data recovery, gearbox and retimer functionality, which convert lanes of data received on line cards or by optical modules into different configurations and/or ensure signal integrity. In the quarter ended September 30, 2017, we notified our customers that we intend to discontinue our LineSpeed IC product line. We are currently supporting existing LineSpeed IC customers and accepting last-time product orders. Going forward, we expect to focus all of our efforts on our Bandwidth Engine IC product line. Historically, our primary business was the design, development, marketing, sale and support of differentiated intellectual property, or IP, including embedded memory and high-speed parallel and SerDes I/O used in advanced systems-on-chips, or SoCs. Our future success and ability to achieve and maintain profitability are dependent on the marketing and sales of our IC products into networking, communications and other markets requiring high-bandwidth memory access.

Historically, our primary business was the design, development, marketing, sale and support of differentiated intellectual property, or IP, including embedded memory and high-speed parallel and SerDes I/O used in advanced systems-on-chips, or SoCs. Currently, we are focused on developing differentiated IP-rich IC products and are dedicating all our research and development, marketing and sales budget to these IC products.

Our future success and ability to achieve and maintain profitability are dependent on the marketing and sales of our IC products into networking, communications and other markets requiring high-bandwidth memory access.

We incurred net losses of approximately $10.1 million and $17.6 million for the nine months ended September 30, 2017 and 2016. We incurred net losses of approximately $32.0 million and $31.5 million for the years ended December 31, 2016 and 2015, respectively, and had an accumulated deficit of approximately $214.0 million as of December 31, 2016. These and prior year losses have resulted in significant negative cash flows for almost a decade and have necessitated that we raise substantial amounts of additional capital during this period. To date, we have primarily financed our operations through multiple offerings of common stock to investors and affiliates, as well as asset sale transactions. In March 2016, we entered into a 10% Senior Secured Convertible Note Purchase Agreement with the purchasers of $8 million principal amount of 10% Senior Secured Convertible Notes due August 15, 2018 (the Notes), at par, in a private placement transaction. The Notes bear interest at the annual rate of 10%. Accrued interest is payable semi-annually in cash or in kind through the issuance of identical new Notes, or with a combination of the two, at our option. Through February 2017, we have made the interest payments in-kind through the issuance of additional notes totaling approximately $0.8 million. Further, the Notes restrict our ability to incur any indebtedness for borrowed money, unless such indebtedness by its terms is expressly subordinated to the Notes in right of payment and to the security interest of the Note holder(s) in respect to the priority and enforcement of any security interest in property of the Company securing such new debt; provided that the Note holder(s) security interest and cash payment rights under the Notes shall be subordinate to a maximum of $5 million of indebtedness for a secured accounts receivable line of credit facility under certain conditions. (See Note No. 11 to our Annual consolidated financial statements, Convertible Notes)

We expect to continue to incur operating losses for the foreseeable future as we secure customers for and continues to invest in the commercialization of our IC products. Due to the strong commitment of our resources to research and development and expansion of its product offerings to customers, we will need to increase revenues substantially beyond levels that we have attained in the past in order to generate sustainable operating profit and sufficient cash flows to continue doing business without raising additional capital from time to time. As a result of our expected operating losses and cash burn for the foreseeable future, recurring losses from operations, and the need to repay the

Notes and accrued interest in 2018, if we are unable to raise sufficient capital through additional debt or equity arrangements, there will be uncertainty regarding our ability to maintain liquidity sufficient to operate our business effectively, which raises substantial doubt as to our ability to continue as a going concern within one year from the date of issuance of our consolidated financial statements. The consolidated financial statements do not include any adjustments that might result from this uncertainty. There can be no assurance that such additional capital, whether in the form of debt or equity financing, will be sufficient or available and, if available, that such capital will be offered on terms and conditions acceptable to us. We are exploring various alternatives, and expect to implement cost reductions to successfully sustain

Table of Contents

the business. If we are unsuccessful in these efforts, we will need to implement significant cost reduction strategies that could affect our near- and long-term business plan. These efforts may include, but are not limited to: reducing headcount and curtailing business activities, especially around new product development.

Critical Accounting Policies and Use of Estimates

Our consolidated financial statements are prepared in conformity with accounting principles generally accepted in the United States of America. Note 1 to the consolidated financial statements describes the significant accounting policies and methods used in the preparation of our consolidated financial statements.

We have identified the accounting policies below as some of the more critical to our business and the understanding of our results of operations. These policies may involve estimates and judgments that affect the reported amounts of assets, liabilities, revenues and expenses. Although we believe our judgments and estimates are appropriate, actual future results may differ from our estimates, and if different assumptions or conditions were to prevail, the results could be materially different from our reported results.

Revenue Recognition

General

We generate revenue from the sales of IC products and licensing of our IP. We recognize revenue when persuasive evidence of an arrangement exists, delivery or performance has occurred, the sales price is fixed or determinable, and collectibility is reasonably assured. Evidence of an arrangement generally consists of signed agreements or customer purchase orders.

IC Products

Products are sold both directly to customers, as well as through distributors. Revenue from sales directly to customers is generally recognized at the time of shipment. We may record an estimated allowance, at the time of shipment, for future returns and other charges against revenue consistent with the terms of sale. IC product revenue and costs relating to sales made through distributors with rights of return or stock rotation are generally deferred until the distributors sell the product to end customers due to our inability to estimate future returns and credits to be issued. Distributors are generally able to return up to 10% of their purchases of slow, non-moving or obsolete inventory for credit every six months. At the time of shipment to distributors, an accounts receivable for the selling price is recorded, as there is a legally enforceable right to receive payment, and inventory is relieved, as legal title to the inventory is transferred upon shipment. Revenues are recognized upon receiving notification from the distributors that products have been sold to end customers. Distributors provide information regarding products and quantity, end customer shipments and remaining inventory on hand. The associated deferred margin is included in the accrued expenses and other line item in the consolidated balance sheets.

Royalty

Royalty revenue represents amounts earned under provisions in our memory licensing agreements that require our licensees to report royalties and make payments at a stated rate based on actual units manufactured or sold by licensees for products that include our memory IP. Our license agreements require the licensee to report the manufacture or sale of products that include our technology after the end of the quarter in which the sale or manufacture occurs. We recognize royalties in the quarter in which we receive the licensee’s report. The timing and level of royalties are difficult to predict, and depend on the licensee’s ability to market, produce and sell products incorporating our technology.

Licensing

Licensing revenue consists of fees earned from license agreements, development services and support and maintenance. For stand-alone license agreements or license deliverables in multi-deliverable arrangements that do not require significant development, modification or customization, revenue is recognized when all revenue recognition

Table of Contents

criteria have been met. Delivery of the licensed technology is typically the final revenue recognition criterion met, at which time revenue is recognized. If any of the criteria are not met, revenue recognition is deferred until such time as all criteria have been met. Support and maintenance revenue is recognized ratably over the period during which the obligation exists, typically 12 months.

Fair Value Measurements of Financial Instruments

We measure the fair value of financial instruments using a fair value hierarchy that prioritizes the inputs to valuation techniques used to measure fair value into three broad levels, as follows:

Level 1—Inputs used to measure fair value are unadjusted quoted prices that are available in active markets for the identical assets or liabilities as of the reporting date.

Level 2—Pricing is provided by third party sources of market information obtained from investment advisors rather than models. We do not adjust for or apply any additional assumptions or estimates to the pricing information we receive from advisors. Our Level 2 securities include cash equivalents and available-for-sale securities, which consisted primarily of corporate debt, and government agency and municipal debt securities from issuers with high quality credit ratings. Our investment advisors obtain pricing data from independent sources, such as Standard & Poor's, Bloomberg and Interactive Data Corporation, and rely on comparable pricing of other securities because the Level 2 securities we hold are not actively traded and have fewer observable transactions. We consider this the most reliable information available for the valuation of the securities.

Level 3—Unobservable inputs that are supported by little or no market activity and reflect the use of significant management judgment are used to measure fair value. These values are generally determined using pricing models for which the assumptions utilize management's estimates of market participant assumptions. The determination of fair value for Level 3 investments and other financial instruments involves the most management judgment and subjectivity.

Valuation of long-lived Assets

We evaluate our long-lived assets for impairment at least annually, or more frequently when a triggering event is deemed to have occurred. This assessment is subjective in nature and requires significant management judgment to forecast future operating results, projected cash flows and current period market capitalization levels. If our estimates and assumptions change in the future, it could result in a material write-down of long-lived assets. We amortize our finite-lived intangible assets, such as developed technology and patent license, on a straight-line basis over their estimated useful lives of three to seven years. We recognize an impairment charge as the difference between the net book value of such assets and the fair value of the assets on the measurement date.

Goodwill

We review goodwill for impairment on an annual basis or whenever events or changes in circumstances indicate the carrying value of an asset may not be recoverable. We first assess qualitative factors to determine whether it is more-likely-than-not that the fair value of the reporting unit is less than the carrying amount as a basis for determining whether it is necessary to perform the two-step impairment test. If the qualitative assessment warrants further analysis, we compare the fair value of the reporting unit to its carrying value. The fair value of the reporting unit is determined using the market approach. If the fair value of the reporting unit exceeds the carrying value of net assets of the reporting unit, goodwill is not impaired, and no further testing is performed. If the carrying value of the reporting unit's goodwill exceeds its implied fair value, then we must record an impairment charge equal to the difference. We have determined that we have a single reporting unit for purposes of performing the goodwill impairment test. We use the

market approach to assess impairment in the second step of the analysis. We performed the annual impairment test in September 2017, and the test did not indicate impairment of goodwill.

During the fourth quarter of 2016, we concluded a triggering event had occurred due to a sustained decrease in the price per share of our common stock and related reduced market capitalization. We performed the first step of the

Table of Contents

impairment test to identify potential goodwill impairment, and the test results indicated the goodwill carrying value was greater than its fair value. We then performed a step-two analysis to compare the carrying amount of goodwill to the implied fair value of the goodwill, and we determined the estimated fair values of the assets and liabilities of its single reporting unit. The fair values of the assets and liabilities identified in the impairment test were determined using the combination of the income approach and the market approach. The implied fair value of goodwill was measured as the excess of the fair value of our single reporting unit over the fair value of its assets and liabilities. As a result of the step-two test, we recorded a non-cash impairment charge of $9,858,000 during the fourth quarter of 2016.

Deferred tax valuation allowance

When we prepare our consolidated financial statements, we estimate our income tax liability for each of the various jurisdictions where we conduct business. This requires us to estimate our actual current tax exposure and to assess temporary differences that result from differing treatment of certain items for tax and accounting purposes. These differences result in deferred tax assets, which we show on our consolidated balance sheet under the category of other current assets. The net deferred tax assets are reduced by a valuation allowance if, based upon weighted available evidence, it is more likely than not that some or all of the deferred tax assets will not be realized. We must make significant judgments to determine our provision for income taxes, our deferred tax assets and liabilities and any valuation allowance to be recorded against our net deferred tax asset.

Stock-based compensation

We recognize stock-based compensation for equity awards on a straight-line basis over the requisite service period, usually the vesting period, based on the grant-date fair value. We estimate the value of employee stock options on the date of grant using the Black-Scholes model. The determination of fair value of share-based payment awards on the date of grant using an option-pricing model is affected by our stock price, as well as assumptions regarding a number of highly complex and subjective variables. These variables include, but are not limited to, the expected stock price volatility over the term of the awards, and actual and projected employee stock option exercise behaviors. The expected term of options granted is derived from historical data on employee exercises and post-vesting employment termination behavior. The expected volatility is based on the historical volatility of our stock price.

Results of Operations for Three and Nine Months

Net Revenue.

	September 30,		Change	
	2017	2016	2016 to 2017	
	(dollar amounts in thousands)			
Product -three months ended	$ 2,231	$ 1,205	$ 1,026	85 %
Percentage of total net revenue	91 %	77 %		
Product -nine months ended	$ 4,297	$ 3,612	$ 685	19 %
Percentage of total net revenue	85 %	78 %		

Product revenue increased for the three and nine months ended September 30, 2017 compared with the same periods of 2016 primarily due to higher shipment volumes of our Bandwidth Engine products.

	September 30,		Change	
	2017	2016	2016 to 2017	
	(dollar amounts in thousands)			
Royalty and other -three months ended	$ 222	$ 368	$ (146)	(40) %
Percentage of total net revenue	9 %	23 %		
Royalty and other -nine months ended	$ 752	$ 1,045	$ (293)	(28) %
Percentage of total net revenue	15 %	22 %		