

AMKOR TECHNOLOGY INC

Form 10-K/A

June 06, 2005

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UNITED STATES SECURITIES AND EXCHANGE COMMISSION
Washington, D.C. 20549

Form 10-K/A

ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d)
OF THE SECURITIES EXCHANGE ACT OF 1934
For the Fiscal Year Ended December 31, 2004

Commission File Number 000-29472

Amkor Technology, Inc.

(Exact name of registrant as specified in its charter)

Delaware
(State of incorporation)

23-1722724
(I.R.S. Employer Identification
Number)

1900 South Price Road
Chandler, AZ 85248
(480) 821-5000

(Address of principal executive offices and zip code)

Securities registered pursuant to Section 12(b) of the Act: None

Securities registered pursuant to Section 12(g) of the Act:
Common Stock, \$0.001 par value

Indicate by check mark whether the registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days. Yes ☒ No ☐

Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K is not contained herein, and will not be contained, to the best of registrant's knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this Form 10-K. ☐

Indicate by check mark whether the registrant is an accelerated filer (as defined in Rule 12b-2 of the Act). Yes ☐ No ☒

The aggregate market value of the voting and non-voting common equity held by non-affiliates computed by reference to the price at which the common equity was last sold as of the last business day of the registrant's most recently completed second fiscal quarter, June 30, 2004, was approximately \$834,369,470.

The number of shares outstanding of each of the issuer's classes of common equity, as of June 1, 2005, was as follows: 176,714,357 shares of Common Stock, \$0.001 par value.

Documents Incorporated by Reference: None.

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We are filing this amendment to our Annual Report on Form 10-K to restate our consolidated financial statements for the years ended December 31, 2002, 2003 and 2004. We previously did not exclude from capital expenditures reported in the consolidated statement of cash flows, capital expenditures that were unpaid and included in accounts payable or accrued expenses at the end of the reporting period. Thus capital expenditures were reported in the consolidated statement of cash flows on an accrual basis rather than on a cash basis which is inconsistent with the requirements of SFAS No. 95, Statement of Cash Flows. This error resulted in an over/understatement of cash flows from investing activities with an equal over/understatement of cash flows from operating activities. This restatement did not impact our previously reported balance sheets or statements of operations (including our net income (loss), earnings (loss) per share or our stockholders' equity). We are also filing amendments to our Quarterly Reports on Form 10-Q for the quarters ended March 31, June 30, and September 30 of 2004 to correct this error.

Based on the Public Company Accounting Oversight Board's definition of material weakness, restatement of financial statements included in prior filings with the SEC is a strong indicator of the existence of a material weakness in the design or operation of internal control over financial reporting. The restatement of our consolidated financial statements as a result of the error described above has led management to conclude that a material weakness existed in our internal control over financial reporting as of December 31, 2004, and that Management's Report on Internal Control over Financial Reporting should also be restated. Accordingly, this amended filing includes a revised Management Report that reflects management's conclusion that the Company's internal control over financial reporting was not effective at December 31, 2004. The report of the Company's independent registered public accounting firm was also revised to reflect their conclusion that the Company's internal control over financial reporting was not effective at December 31, 2004. In accordance with the rules of the SEC, the affected items of the Form 10-K, Items 6, 7, 8 and 9A of Part II, are being amended.

No attempt has been made in this Form 10-K/A to update other disclosures presented in the original report on Form 10-K, except as required to reflect the effects of the restatement. This Form 10-K/A does not reflect events occurring after the filing of the 2004 Form 10-K or modify or update those disclosures, including the exhibits to the Form 10-K affected by subsequent events; however, this Form 10-K/A includes as exhibits 31.1, 31.2 and 32 new certifications by our principal executive officer and principal financial officer as required by Rule 12b-15 promulgated under the Securities Exchange Act of 1934, as amended. Accordingly, this Form 10-K/A should be read in conjunction with our filings made with the SEC subsequent to the filing of the original Form 10-K for the year ended December 31, 2004, including any amendments to those filings.

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All references in this Annual Report to Amkor, we, us, our or the company are to Amkor Technology, Inc. and its subsidiaries. We refer to the Republic of Korea, which is also commonly known as South Korea, as Korea. All references in this Annual Report to ASI are to Anam Semiconductor, Inc. and its subsidiaries. As of December 31, 2004, we owned 2% of ASI's outstanding voting stock. PowerQuad, SuperBGA, *FlexBGA*, ChipArray, PowerSOP, *MicroLeadFrame*, ETCSP, TapeArray, VisionPak and Amkor Technology are trademarks or registered trademarks of Amkor Technology, Inc. All other trademarks appearing herein are held by their respective owners. Digital Light Processing is a registered trademark of Texas Instruments, Inc.

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PART I

Item 1. *Business*

DISCLOSURE REGARDING FORWARD-LOOKING STATEMENTS

This business section contains forward-looking statements. In some cases, you can identify forward-looking statements by terminology such as may, will, should, expects, plans, anticipates, believes, estimates, potential, continue or the negative of these terms or other comparable terminology. These statements are only predictions. Actual events or results may differ materially. In evaluating these statements, you should specifically consider various factors, including the risks outlined under Management's Discussion and Analysis of Financial Condition and Results of Operations Risk Factors that May Affect Future Operating Performance in Item 7 of this Annual Report. These factors may cause our actual results to differ materially from any forward-looking statement.

OVERVIEW

Amkor is one of the world's largest subcontractors of semiconductor packaging and test services. Amkor pioneered the outsourcing of semiconductor packaging and test services in 1968, and over the years has built a leading position by:

Providing a broad portfolio of packaging and test technologies and services,

Maintaining a leading role in the design and development of new package and test technologies,

Cultivating long-standing relationships with customers, including many of the world's leading semiconductor companies,

Developing expertise in high-volume manufacturing; and

Providing a broadly diversified operational scope, with production capabilities in China, Korea, Japan, the Philippines, Singapore, Taiwan and the U.S.

The semiconductors that we package and test for our customers ultimately become components in electronic systems used in communications, computing, consumer, industrial and automotive applications. Our customers include, among others, Agilent Technologies, Atmel Corporation, International Business Machines Corp. (IBM), Infineon Technologies AG, Intel Corporation, Philips Electronics N.V., Samsung, ST Microelectronics PTE, Sony Semiconductor Corporation, Texas Instruments and Toshiba Corporation. The outsourced semiconductor packaging and test market is very competitive. We also compete with the internal semiconductor packaging and test capabilities of many of our customers.

Packaging and test are integral parts of the semiconductor manufacturing process. Semiconductor manufacturing begins with silicon wafers and involves the fabrication of electronic circuitry into complex patterns, thus creating individual chips on the wafers. The packaging process creates an electrical interconnect between the semiconductor chip and the system board. In packaging, the fabricated semiconductor wafers are cut into individual chips which are attached to a substrate and then encased in a protective material to provide optimal electrical connectivity and thermal performance. The packaged chips are then tested using sophisticated equipment to ensure that each packaged chip meets its design specifications. Increasingly, packages are custom designed for specific chips and specific end-market applications.

Website Access to SEC Reports

We maintain an Internet website at www.amkor.com. Our periodic SEC reports (including Annual Reports on Form 10-K, Quarterly Reports on Form 10-Q, Current Reports on Form 8-K and amendments to those reports filed or furnished pursuant to Section 13(a) or 15(d) of the Exchange Act) are accessible through our website, free of charge, as soon as reasonably practicable after such reports are filed electronically with or furnished to the SEC. To access these reports, go to our website at www.amkor.com/ir.

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INDUSTRY BACKGROUND

Semiconductor devices are the essential building blocks used in most electronic products. As semiconductor devices have evolved, there have been three important consequences: (1) an increase in demand for computers and consumer electronics fostered by declining prices for such products; (2) the proliferation of semiconductor devices into diverse end products such as consumer electronics, communications equipment and automotive systems; and (3) an increase in the semiconductor content in electronic products. These consequences have fueled the growth of the overall semiconductor industry, as well as the market for outsourced semiconductor assembly and test services.

Outsourcing Trends

Historically, semiconductor companies packaged semiconductors primarily in their own factories and relied on subcontract providers to handle overflow volume. In recent years, semiconductor companies have increasingly outsourced their packaging and testing to subcontract providers, such as us, for the following reasons:

Subcontract providers have developed expertise in advanced packaging and test technologies.

Semiconductor companies are facing increasing demands for miniaturization and improved thermal and electrical performance in semiconductor devices. This trend, along with increasing complexity in the design of semiconductor devices and the increased customization of interconnect packages, has led many semiconductor companies to view packaging and test as an enabling technology requiring sophisticated expertise and technological innovation. As packaging and test technology becomes more advanced, many semiconductor companies have had difficulty developing adequate internal packaging and test capabilities and are relying on subcontract providers of packaging and test services as a key source of new package design and production.

Subcontract providers can offer shorter time to market for new products because their resources are dedicated to packaging and test solutions.

We believe that semiconductor companies are seeking to shorten the time to market for their new products, and that having the appropriate packaging technology and capacity in place is a critical factor in facilitating product introductions.

Semiconductor companies frequently do not have sufficient time to develop their packaging and test capabilities or deploy the equipment and expertise to implement new packaging technology in volume. For this reason, semiconductor companies are leveraging the resources and capabilities of subcontract packaging and test companies to deliver their new products to market more quickly.

Many semiconductor manufacturers do not have the economies of scale to offset the significant costs of building packaging and test factories.

Semiconductor packaging is a complex process requiring substantial investment in specialized equipment and factories. As a result of the large capital investment required, this manufacturing equipment must operate at a high capacity level for an extended period of time to be cost effective. Shorter product life cycles, faster introductions of new products and the need to update or replace packaging equipment to accommodate new package types have made it more difficult for semiconductor companies to maintain cost effective utilization of their packaging and test assets. Subcontract providers of packaging and test services, on the other hand, can use their equipment to support a broad range of customers, potentially generating greater manufacturing economies of scale.

The availability of high quality packaging and testing from subcontractors allows semiconductor manufacturers to focus their resources on semiconductor design and wafer fabrication.

As semiconductor process technology migrates to larger wafers and smaller feature size, a state-of-the-art wafer fabrication facility can cost in excess of \$2 billion. Subcontractors have demonstrated the ability to deliver advanced packaging and test solutions at a competitive price, thus allowing semiconductor companies to focus their capital resources on core wafer fabrication activities rather than invest in advanced packaging and test technology.

There are many semiconductor companies without factories, known as fabless companies, which design semiconductor chips and outsource all of the associated manufacturing.

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Fabless semiconductor companies focus exclusively on the semiconductor design process and outsource virtually every step of the manufacturing process. We believe that fabless semiconductor companies will continue to be a significant driver of growth in the subcontract packaging and test industry.

These outsourcing trends, combined with the growth in the number of semiconductor devices being produced and sold, are increasing demand for subcontracted packaging and test services. Today, nearly all of the world's major semiconductor companies use packaging and test service subcontractors for at least a portion of their packaging and test needs.

COMPETITIVE STRENGTHS

We believe our competitive strengths include the following:

Broad Offering of Package Design, Packaging and Test Services

Integrating advanced semiconductor technology into electronic end products often poses unique thermal and electrical challenges, and Amkor employs a large number of design engineers to create package formats that solve these challenges. Amkor produces more than 1,000 package types, representing one of the broadest package offerings in the semiconductor industry. We provide customers with a wide array of packaging alternatives including leadframe and laminate packages, in both wirebond and flip chip formats. We are also a leading assembler of complementary metal oxide silicon (CMOS) image sensor devices used in digital cameras and cellular phones, and micro-electromechanical system (MEMS) devices used in a variety of end markets, including automotive, industrial and personal entertainment. We also offer an extensive line of services to test analog, digital, logic, mixed signal and radio frequency semiconductor devices. We believe that the breadth of our design, packaging and test services is important to customers seeking to reduce the number of their suppliers.

Leading Technology Innovator

We believe that we are one of the leading providers of advanced wafer bumping, and semiconductor packaging and test solutions. We have designed and developed several state-of-the-art leadframe and laminate package formats including our *MicroLeadFrame*, *VisionPak*, *PowerQuad*, *SuperBGA*, *flexBGA* and *ChipArray* BGA packages. Through Unitive, Inc. and Unitive Semiconductor Taiwan, companies that we acquired in August 2004, we offer advanced, electroplated wafer bumping and wafer level processing technologies. To maintain our leading industry position, we have more than 350 employees engaged in research and development focusing on the design and development of new semiconductor packaging and test technologies. We work closely with customers and technology partners to develop new and innovative package designs.

Long-Standing Relationships With Prominent Semiconductor Companies

Our customer base consists of more than 300 companies, including most of the world's largest semiconductor companies. Over the last three decades Amkor has developed long-standing relationships with many of our customers. In 2004, we entered into a long-term supply agreement with IBM in which we expect to provide a substantial majority of IBM's outsourced semiconductor packaging and test. In addition, we are the sole outsourced packaging and test partner for digital micro-mirror devices used in Texas Instrument's Digital Light ProcessingTM systems.

Advanced Manufacturing Capabilities

We believe that our manufacturing excellence has been a key factor in our success in attracting and retaining customers. We have worked with our customers and our suppliers to develop proprietary process technologies to

enhance our existing manufacturing capabilities, reduce time to market, increase quality and lower manufacturing costs. We believe our manufacturing cycle times are among the fastest available from any subcontractor of packaging and test services.

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Geographically Diversified Operational Base

Since 2000, we have expanded our historical base of assembly and test operations in Korea and the Philippines to include China, Japan, Singapore, Taiwan and the U.S., and as a result we now have a broad geographical manufacturing base.

COMPETITIVE DISADVANTAGES

You should be aware that our competitive strengths may be diminished or eliminated due to certain challenges faced by us and which our principal competitors may not face, including the following:

High Leverage We have substantial indebtedness, and the associated interest expense significantly increases our cost structure. Our substantial indebtedness could limit our ability to fund future working capital, capital expenditures, research and development and other general corporate requirements.

Difficulties Integrating Acquisitions During 2004, we acquired test operations from IBM located in Singapore and acquired Unitive, Inc. and Unitive Semiconductor Taiwan. We face challenges as we integrate new and diverse operations and try to attract qualified employees to support our expansion plans.

In addition, we and our competitors face a variety of operational and industry risks inherent to the industry in which we operate. For a complete discussion of risks associated with our business, please read **Management's Discussion and Analysis of Financial Condition and Results of Operations - Risk Factors that May Affect Future Operating Performance** in Item 7 of this Annual Report.

STRATEGY

To build upon our industry position and to remain a preferred subcontractor of semiconductor packaging and test services, we are pursuing the following strategies:

Capitalize on Outsourcing Trend

We believe that notwithstanding a tendency for outsourcing to slow during industry downturns, there remains a long-term trend towards more outsourcing on the part of semiconductor companies. We believe that many vertically integrated semiconductor companies reduce their investments in advanced packaging and test technology during industry downturns and increase their reliance on outsourced packaging and test suppliers for advanced package and test requirements. We also believe that as the semiconductor content of electronic end products increases in complexity, so will the need for the advanced package and test solutions. Accordingly, we expect semiconductor companies will expand their outsourcing of advanced semiconductor packaging and test services and we intend to capitalize on this growth. We believe semiconductor companies will increasingly outsource packaging and test services to companies who can provide advanced technology and high-quality, high-volume manufacturing expertise.

Leverage Scale and Scope of Packaging and Test Capabilities

We are committed to accommodating the long-term outsourcing trend by expanding the scale of our operations and the scope of our packaging and test services. We believe that our scale and scope allow us to provide cost-effective solutions to our customers in the following ways:

We have the capacity to absorb large orders and accommodate quick turn-around times,

We use our size and industry position to obtain favorable pricing on materials and manufacturing equipment, and

We offer an exceptionally broad range of packaging and test services and can serve as the primary supplier of such services for many of our customers.

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Maintain Our Technology Leadership

We intend to continue to develop and commercialize leading-edge packaging technologies, including flip chip, system-in-package, package-on-package, stacked chip scale and wafer level packaging. We believe that our focus on research and product development will enable us to enter new markets early, capture market share and promote the adoption of our new package designs as industry standards. We seek to enhance our in-house research and development capabilities through the following activities:

Collaborating with integrated device manufacturer customers, or IDM customers, to gain access to technology roadmaps for next generation semiconductor designs and to develop new packages that satisfy their future requirements,

Collaborating with original equipment manufacturers, or OEMs, such as Toshiba Corporation, Cisco Systems, Sony Ericsson Corporation and Nokia Group, to design new packages that function with the next generation of electronic products, and

Collaborating with wafer foundry companies on future package needs for new wafer technologies.

Broaden the Geographical Scope of our Manufacturing Base

Prior to 2001, our manufacturing operations were centered in Korea and the Philippines. In order to diversify our operational footprint and better serve our customers, we adopted a strategy of expanding our operational base to key microelectronic manufacturing areas of Asia. During 2001, we commenced a joint venture with Toshiba Corporation in Japan and we established a manufacturing presence in Taiwan and China. Our goal is to continue to build operational scale in these new geographic locations and capitalize on growth opportunities in their respective markets. In January 2004, we purchased the remaining interest in our joint venture from Toshiba Corporation and, as of that date, we now own 100% of the operation. In May 2004, we acquired from IBM a testing facility in Singapore. In August 2004 we acquired Unitive, Inc. (Unitive), and approximately 60% of Unitive Semiconductor Taiwan Corporation (UST), leading providers of wafer bumping and wafer level packaging services, with operations in North Carolina and Taiwan, respectively.

Provide Integrated, Turnkey Solutions

We are able to provide a turnkey solution including semiconductor wafer bump, wafer probe, wafer backgrind, package design, packaging, test and drop shipment services. We believe that this capability facilitates the outsourcing model by enabling our customers to achieve faster time to market for new products and improved cycle times.

Strengthen Customer Relationships

We intend to enhance our long-standing customer relationships and develop collaborative supply agreements. We believe that because of today's shortened technology life cycles, integrated communications are crucial to speed time to market. We have customer support personnel located near the facilities of major customers and in acknowledged technology centers. These support personnel work closely with customers to plan production for existing packages as well as to develop requirements for the next generation of packaging technology. In addition, we implement direct electronic links with our customers to enhance communication and facilitate the flow of real-time engineering data and order information.

Pursue Strategic Acquisitions

We evaluate candidates for strategic acquisitions and joint ventures to strengthen our business and expand our geographic reach. We believe that there are opportunities to acquire in-house packaging operations of our customers

and competitors. To the extent we acquire operations of our customers, we intend to structure any such acquisition to include long-term supply contracts with those customers. For example, in May 2004 we acquired the Singapore test operations of IBM and contemporaneously entered into a long-term supply agreement with IBM. Under this long-term supply agreement, we will receive a substantial majority of IBM's outsourced semiconductor assembly and test business through 2010.

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We offer a broad range of package formats designed to provide our customers with a full array of packaging solutions. Our packages are divided into two families: traditional, which includes principally traditional leadframe products, and advanced packages, which includes principally advanced leadframes and laminate products.

In response to the increasing demands of today's high-performance electronic products, semiconductor packages have evolved from traditional leadframe packages and now include advanced leadframe and laminate formats. The differentiating characteristics of these package formats include (1) the size of the package, (2) the number of electrical connections the package can support, (3) the thermal and electrical characteristics of the package, and (4) in the case of our System-in-Package family of laminate packages, the integration of multiple active and passive components in a single package.

As semiconductor devices increase in complexity, they often require a larger number of electrical connections. Leadframe packages are so named because they connect the electronic circuitry on the semiconductor device to the system board through leads on the perimeter of the package. Our laminate products, typically called ball grid array or BGA, use balls on the bottom of the package to create the electrical connections. This array format can support larger numbers of electrical connections.

Evolving semiconductor technology has allowed designers to increase the level of performance and functionality in portable and handheld electronics products, and this has led to the development of smaller package sizes. In leading-edge packages, the size of the package is reduced to approximately the size of the individual chip itself in a process known as chip scale packaging.

The following table sets forth by product type, for the periods indicated, the amount of our packaging and test net revenues in millions of dollars and the percentage of such net revenues:

	Year Ended December 31,					
	2004		2003		2002	
	(Dollars in millions)					
Traditional packages	\$ 352	18.5%	\$ 340	21.2%	\$ 391	27.8%
Advanced packages	1,367	71.9	1,124	70.1	915	65.1
Test	182	9.6	140	8.7	100	7.1
Total packaging and test net revenues	\$ 1,901	100.0%	\$ 1,604	100.0%	\$ 1,406	100.0%

Our packaging and test business operates with no material backlog.

Traditional Packages

Traditional leadframe-based packages are the most widely used package family in the semiconductor industry and are typically characterized by a chip encapsulated in a plastic mold compound with metal leads on the perimeter. Two of our most popular traditional leadframe package types are SOIC and QFP, which support a wide variety of device types and applications. The traditional leadframe package family has evolved from through hole design, where the leads are plugged into holes on the circuit board to surface mount design, where the leads are soldered to the surface

of the circuit board. We offer a wide range of lead counts and body sizes to satisfy variations in the size of customers semiconductor devices.

Advanced Packages

Advanced Leadframe Packages

Through a process of continuous engineering and customization, we have designed several advanced leadframe package types that are thinner and smaller than traditional leadframe packages, with the ability to accommodate more leads on the perimeter of the package. These advanced leadframe packages typically have superior thermal and electrical characteristics, which allow them to dissipate heat generated by high-powered semiconductor devices while providing enhanced electrical connectivity. We plan to continue to develop increasingly smaller versions of these packages to keep pace with continually shrinking semiconductor device sizes and demand for miniaturization of portable electronic products.

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One of our most successful advanced leadframe package offerings is the *MicroLeadFrame*® family of QFN, or Quad Flat No-lead packages. This package family is particularly well suited for radio frequency (RF) and wireless applications. Our smallest *MicroLeadFrame*® package design is less than 2mm square and can fit on the head of a pin.

Laminate Packages

The laminate family employs the ball grid array design, which utilizes a plastic or tape laminate substrate rather than a leadframe substrate, and places the electrical connections on the bottom of the package rather than around the perimeter.

The ball grid array format was developed to address the need for higher lead counts required by many advanced semiconductor devices. As the number of leads on leadframe packages increased, leads were placed closer to one another in order to maintain the small size of the package. The increased lead density resulted in shorting and other electrical challenges, and required the development of increasingly sophisticated and expensive techniques for producing circuit boards to accommodate the high number of leads.

The ball grid array format solved this problem by effectively creating leads on the bottom of the package in the form of small bumps or balls that can be evenly distributed across the entire bottom surface of the package, allowing greater distance between the individual leads.

Our first package format in this family was the plastic ball grid array (PBGA). We have subsequently designed or licensed additional ball grid array package formats that have superior performance characteristics and features that enable low-cost, high-volume manufacturing. These laminate products include:

SuperBGA®, which includes a copper layer to dissipate heat and is designed for low-profile, high-power applications, and

TEPBGA-2, which is a standard PBGA with thicker copper layers plus an integrated heat slug and is designed for enhanced thermal performance in high power applications.

We have also designed a variety of packages, commonly referred to as chip scale packages, or CSP, which are not much larger than the chip itself. Chip scale packages are becoming widely adopted as designers and manufacturers of consumer electronics seek to achieve higher levels of performance while shrinking the product size. Some of our chip scale packages include:

ChipArray®BGA and TapeArray BGA, in which the package is only 1.5 mm larger than the chip itself, and

Wafer Level Package, which further reduces package size and increases manufacturing efficiency.

Advances in packaging technology now allow the placing of two or more chips on top of each other within an individual package. This concept, known as stacked packaging, permits a higher level of semiconductor density and more functionality. In addition, advance wafer thinning technology has fostered the creation of extremely thin packages that can be placed on top of each other within standard height restrictions used in microelectronic system boards. Some of our stacked packages include:

Stacked CSP (S-CSP), which is similar to our ChipArray®BGA, except that S-CSP contains two or more chips placed on top of each other, and

Package-on-package (POP), which are extremely thin chip scale packages that can be stacked on top of each other.

Other Advanced Packages

Our customers are creating smaller and more powerful versions of semiconductor devices to meet demands for miniaturization of portable electronic products, higher performance applications and converging functionality. For many of these devices, the optimal packaging solutions use solder bumps instead of gold wire to form the electrical interconnect between the device and the package. These forms of packaging are called flip chip and wafer level packaging. We offer our customers turnkey flip chip solutions, including wafer probe, wafer bump, assembly, test and drop ship, on 200mm and 300mm wafers. An increasing number of devices, from diodes to DRAMs, use wafer level packaging. Most of these devices are small in size, with hundreds or thousands fabricated on each wafer. Our Wafer Level Chip Scale Packaging (WLCSP)

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service allows chip designers to integrate more technology at the wafer level, on a smaller footprint and with exceptional performance and reliability.

To capitalize on customer demand for higher levels of system integration, we created our System-in-Package (SiP) modules. SiP modules integrate various system elements into a single-function block, thus enabling space and power efficiency, high performance and lower production costs. Most of our SiP packages are laminate based. Our SiP technology is being used to produce a variety of devices including power amplifiers for cellular phones and other portable communication devices, wireless local area network (WLAN) modules for networking applications, memory cards and sensors, such as fingerprint recognition devices.

In order to accommodate the emerging use of digital imaging in a variety of consumer products, we developed VisionPak , a family of CMOS image sensor-based packages that can be incorporated in such products as cellular phones, PDAs, digital cameras and PCs.

We are also a leading outsourced provider of packages based on MEMS that are used in a broad range of industrial and consumer applications, including automobiles and home entertainment.

Test Services

Amkor provides a complete range of test solutions including wafer probe, final test, strip test, marking, bake, drypack, and tape and reel. The devices we test encompass nearly all technologies produced in the industry today including digital, linear, mixed signal, memory, RF and integrated combinations of these technologies. In 2004, we tested over 2.4 billion units making us one of the highest volume testing companies in the subcontract packaging and test business. We tested 33%, 28% and 21% of the units that we packaged in 2004, 2003 and 2002, respectively. Historically, our test operations have been co-located within our packaging factories. In 2004, we acquired the Singapore test operations of IBM, including a 141,000 square foot leased facility.

We are also an industry leader in providing innovative testing solutions that help to lower the total cost of test for our customers. Two examples of these innovative approaches are strip test and low cost RF test. Strip test involves parallel testing, in which large numbers of packaged units can be tested at one time, as compared to singulated testing in which individual packaged units are tested. With strip test, electronically isolated packaged units are tested in parallel, resulting in faster handler index times and higher throughput rates, thus reducing test cost and increasing test yield. In 2004, we strip tested approximately 735 million units.

In the area of low cost RF test, we have developed one of the lowest cost test solutions in the industry for testing simple RF devices that are pervasive in today's cell phones and WLAN products. This test approach combines inexpensive test hardware with integration software to achieve test costs that are significantly less costly than industry standard test practices. We believe that our low cost RF test technology provides a competitive advantage for us and, when it is combined with our System-in-Package and *MicroLeadFrame*® packaging technologies, offers our customers one of the industry's lowest total cost solutions.

We also provide value added engineering services in addition to basic device testing. These services include test program development, test hardware development, test program conversion to lower cost test systems, device characterization and reliability qualification testing. In total, we can provide all of the test engineering services needed by our customers to get their products ready for high volume production. We believe that this service will continue to become more valuable to our customers as they face resource constraints not only in their production testing, but also in their test engineering and development areas.

In 2003, we strengthened our test operations in Taiwan and mainland China by entering into strategic alliances in each of these countries. We entered into these alliances in order to enhance our ability to provide test support for our growing packaging business and to provide our customers broader and more rapidly scalable test capacity.

WAFER FABRICATION SERVICES

In January 1998, we entered into a supply agreement with ASI to market wafer fabrication services provided by ASI's semiconductor wafer fabrication facility using 0.35 micron, 0.25 micron and 0.18 micron CMOS process technology provided by Texas Instruments pursuant to technology assistance agreements with ASI. On February 28, 2003, we sold our wafer fabrication services business to ASI. Additionally, we obtained a release from Texas Instruments regarding our

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contractual obligations with respect to wafer fabrication services to be performed subsequent to the transfer of the business to ASI. We have restated our historical results to reflect our wafer fabrication services segment as a discontinued operation for all periods presented. In connection with the disposition of our wafer fabrication business, we recorded, in the first quarter of 2003, \$1.0 million in severance and other exit costs to close our wafer fabrication services operations in Boise, Idaho and Lyon, France. Also in the first quarter of 2003, we recognized a pre-tax gain on the disposition of our wafer fabrication services business of \$58.6 million (\$51.5 million, net of tax).

RESEARCH AND DEVELOPMENT

Our research and development efforts focus on developing new package products and improving the efficiency and capabilities of our existing production processes. We believe that technology development is one of the key success factors in the semiconductor packaging and test market and also believe that we have a distinct advantage in this area. Our focus on research and development efforts enable us to enter markets early, capture market share and promote the adoption of our new package offerings as industry standards. These efforts also support our customers' needs for smaller packages, increased performance, and lower cost. In addition, we license our leading edge technology, such as *MicroLeadFrame*®, to customers and competitors. We continue to invest our research and development resources to further the development of flip chip interconnection solutions, chip scale and stack packages, *MicroLeadFrame*® and System-in-Package technologies.

As of December 31, 2004, we had more than 350 employees in research and development activities. In addition, we involve management and operations personnel in research and development activities. In 2004, 2003 and 2002, we spent \$36.7 million, \$30.2 million and \$35.9 million, respectively, on research and development.

MARKETING AND SALES

Our marketing offices manage and promote our packaging and test services while key customer and technical support is provided through our network of international sales offices. To better serve our customers, our offices are located near our largest customers or areas where there is customer concentration. Our marketing and sales office locations include sites in the U.S. (Chandler, Arizona; Irvine, Santa Clara and San Diego, California; Boston, Massachusetts; Greensboro, North Carolina; West Chester, Pennsylvania, and Austin and Dallas, Texas), Cayman Islands, China, France, Japan, Korea, the Philippines, Singapore, Taiwan and the United Kingdom.

To provide comprehensive sales and customer service, we assign each of our customers a direct support team consisting of an account manager, technical program manager, test program manager and both field and factory customer support representatives. We also support our largest multinational customers from multiple office locations to ensure that we are aligned with their global operational and business requirements.

Our direct support teams are further supported by an extended staff of product, process, quality and reliability engineers, as well as marketing and advertising specialists, information systems technicians and factory personnel. Together, these direct and extended support teams deliver an array of services to our customers. These services include:

Managing and coordinating ongoing manufacturing activity,

Providing information and expert advice on our portfolio of packaging and test solutions and related trends,

Managing the start-up of specific packaging and test programs thus improving customers' time to market,

Providing a continuous flow of information to our customers regarding products and programs in process,

Partnering with customers on concurrent design solutions,

Researching and assisting in the resolution of technical and logistical issues,

Aligning our technologies and research and development activities with the needs of our customers and OEMs,

Providing guidance and solutions to customers in managing their supply chains,

Driving industry standards,

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Providing design and simulation services to insure package reliability, and

Collaborating with our customers on continuous quality improvement initiatives.

Further, we implement direct electronic links with our customers to:

Achieve near real time and automated communications of order fulfillment information, such as inventory control, production schedules and engineering data, such as production yields, device specifications and quality indices, and

Connect our customers to our sales and marketing personnel worldwide and to our factories.

Web-enabled tools provide our customers real time access to the status of their products, the performance of our manufacturing lines, and technical data they require to support their new product introductions.

CUSTOMERS

As of February 28, 2005, we had more than 300 customers, including many of the largest semiconductor companies in the world. The table below lists our top 50 customers in 2004 based on revenues:

AMI Semiconductor, Inc.	Motorola, Inc.
Agere Technologies, Inc.	MStar Semiconductor, Inc.
Agilent Technologies	MTEKVISION Co., Ltd.
Altera Corporation	National Semiconductor Corporation
Analog Devices, Inc.	NEC Corporation Ltd.
Atmel Corporation	Nvidia Corporation
Austria Mikro Systeme	PMC - Sierra Inc.
Broadcom Corporation	Philips Electronics
Conexant Systems Inc.	Realtek Semiconductor Corporation
Core Logic Inc.	Renesas Technology (Hitachi)
eSilicon Corp.	R.F Micro Devices
ESS Technology Inc.	Ricoh Co., Ltd.
Fairchild Semiconductor Corporation	Robert Bosch GmbH
Infineon Technologies AG	Samsung Electronics Corporation, Ltd.
Integrated Device Technology, Inc.	Sanyo Electric Co., Ltd.
Intel Corporation	Silicon Image, Inc.
International Business Machines Corporation	Silicon Laboratories Inc.
Intersil Corporation	Skyworks Solutions, Inc.
Lattice Semiconductor Corporation	Sony Semiconductor Corporation
LSI Logic Corporation	SST International Ltd
Macronix International Co., Ltd.	ST Microelectronics PTE
Maxim Integrated Circuits	Standard Microsystems
Mediatek Inc.	Texas Instruments, Inc.
Microchip Technology Inc.	Toshiba Corporation
Micronas Semiconductor Holding AG	Xilinx, Inc

Our services are available internationally. A summary of our domestic and international net revenue and net property, plant and equipment is set forth in Note 22 to the Consolidated Financial Statements in Item 8, which is incorporated herein by reference to this Annual Report on Form 10-K. More than half of our overall net revenue comes from outside of the United States.

For a discussion of risks attendant to our foreign operations, see Management's Discussion and Analysis of Financial Condition and Results of Operations Risk Factors That May Affect Future Operating Performance Risks Associated with International Operations We Depend on Our Factories in China, Japan, Korea, the Philippines, Singapore and Taiwan. Many of Our Customers and Vendors Operations Are Also Located Outside of the U.S. in Item 7 of this Annual Report.

With the commencement of operations of Amkor Iwate and the acquisition of a packaging and test facility from Toshiba in 2001, total net revenues derived from Toshiba accounted for 11.6% and 14.7% of our consolidated net revenues for 2003

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and 2002, respectively. Total net revenues derived from Toshiba were less than 10% in 2004. During 2004 Amkor's top five customers, including Toshiba, accounted for 26% of revenue. Prior to the sale of our wafer fabrication services business to ASI in February 2003, we derived substantially all of our wafer fabrication revenues from Texas Instruments (TI), which due to our restatement, are no longer included in net revenues, but rather, as part of discontinued operations in the restated Consolidated Statements of Operations.

MATERIALS AND EQUIPMENT

Our packaging operations depend upon obtaining adequate supplies of materials and equipment on a timely basis. The principal materials used in our packaging process are leadframes or laminate substrates, gold wire and mold compound. We purchase materials based on customer forecasts, and our customers are generally responsible for any unused materials which we purchased based on such forecasts.

We work closely with our primary material suppliers to insure that materials are available and delivered on time. Moreover, we also negotiate worldwide pricing agreements with our major suppliers to take advantage of the scale of our operations. We are not dependent on any one supplier for a substantial portion of our material requirements.

Our packaging operations depend on obtaining adequate supplies of manufacturing equipment on a timely basis. We work closely with major equipment suppliers to insure that equipment is delivered on time and that the equipment meets our stringent performance specifications.

For a discussion of additional risks associated with our materials and equipment suppliers, see Management's Discussion and Analysis of Financial Condition and Results of Operations—Risk Factors that May Affect Future Operating Performance in Item 7 of this Annual Report.

ENVIRONMENTAL MATTERS

The semiconductor packaging process uses chemicals and gases and generates byproducts that are subject to extensive governmental regulations. For example, at our foreign manufacturing facilities, we produce liquid waste when silicon wafers are diced into chips with the aid of diamond saws, then cooled with running water. Federal, state and local regulations in the United States, as well as environmental regulations internationally, impose various controls on the storage, handling, discharge and disposal of chemicals used in our manufacturing processes and on the factories we occupy.

We have been engaged in a continuing program to assure compliance with federal, state and local environmental laws and regulations. We currently do not expect capital expenditures or other costs attributable to compliance with environmental laws and regulations to have a material adverse effect on our business, results of operations or financial condition.

For a discussion of additional risks associated with the environmental issues, see Management's Discussion and Analysis of Financial Condition and Results of Operations—Risk Factors that May Affect Future Operating Performance—Environmental Regulations in Item 7 of this Annual Report.

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COMPETITION

The subcontracted semiconductor packaging and test market is very competitive. We face substantial competition from established packaging and test service providers primarily located in Asia, including companies with significant manufacturing capacity, financial resources, research and development operations, marketing and other capabilities. These companies include Advanced Semiconductor Engineering, Inc. and its subsidiary ASE Test Limited, ASAT Ltd., STATS ChipPAC Ltd and Siliconware Precision Industries Co., Ltd. Such companies have also established relationships with many large semiconductor companies that are current or potential customers of Amkor. We also compete with the internal semiconductor packaging and test capabilities of many of our customers.

The principal elements of competition in the subcontracted semiconductor packaging market include: (1) price, (2) available capacity, (3) quality, (4) breadth of package offering, (5) technical competence, (6) new package design and implementation, (7) manufacturing cycle times and (8) customer service. We believe that we generally compete favorably with respect to each of these factors.

INTELLECTUAL PROPERTY

Acquisition of Intellectual Property Rights

We maintain an active program to protect our investment in technology by acquiring intellectual property protection and enforcing our intellectual property rights. Intellectual property rights that apply to our various products and services include patents, copyrights, trade secrets and trademarks. We have filed and obtained a number of patents in the U.S. and abroad. While our patents are an important element of our intellectual property strategy and our success, as a whole we are not materially dependent on any one patent or any one technology. We expect to continue to file patent applications when appropriate to protect our proprietary technologies, but we cannot assure you that we will receive patents from pending or future applications. In addition, any patents we obtain may be challenged, invalidated or circumvented and may not provide meaningful protection or other commercial advantage to us.

We also protect certain details about our processes, products and strategies as trade secrets, keeping confidential the information that we believe provides us with a competitive advantage. We have ongoing programs designed to maintain the confidentiality of such information. Further, to distinguish our products from our competitors' products, we have obtained certain trademarks and trade names. We have promoted and will continue to promote our particular product brands through advertising and other marketing techniques.

Enforcement of Intellectual Property Rights

We may need to enforce our patents or other intellectual property rights or defend ourselves against claimed infringement of the rights of others through litigation, which could result in substantial cost and diversion of our resources (for example, refer to our Carsem litigation matter in Item 3. Legal Proceedings). We intend to license our intellectual property when it makes economic sense for us to do so, consistent with the licensing policies of the various domestic and international standards setting organizations of which we are a member. The semiconductor industry is characterized by frequent claims regarding patent and other intellectual property rights. If any third party makes an enforceable infringement claim against us, we could be required to:

discontinue the use of certain processes,

cease the manufacture, use, import and sale of infringing products,

pay substantial damages,

develop non-infringing technologies, or

acquire licenses to the technology we had allegedly infringed.

If we fail to obtain necessary licenses or if we are subjected to litigation relating to patent infringement or other intellectual property matters, our business could suffer.

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As of December 31, 2004, we had 22,033 full-time employees. Of the total employee population, 17,614 were engaged in manufacturing, 2,444 were engaged in manufacturing support, 369 were engaged in research and development, 548 were engaged in marketing and sales and 1,058 were engaged in finance, business management and administration. We believe that our relations with our employees are good. We have never experienced a work stoppage in any of our factories. Our employees in the U.S., China, the Philippines, Singapore and Taiwan are not represented by a collective bargaining unit. Certain members of our factories in Korea and Japan are members of a union, and all employees at these factories are subject to collective bargaining agreements.

Item 2. *Properties*

We provide packaging and test services through our factories in China, Japan, Korea, the Philippines, Singapore, Taiwan and the United States. We believe that total quality management is a vital component of our advanced manufacturing capabilities. We have established a comprehensive quality operating system designed to: (1) promote continuous improvements in our products and (2) maximize manufacturing yields at high volume production without sacrificing the highest quality standards. The majority of our factories are ISO9001:2000, ISO9002, ISO14001 and QS9000 certified. Additionally, as we acquire or construct additional factories, we commence the quality certification process to meet the certification standards of our existing facilities. We believe that many of our customers prefer to purchase from quality certified suppliers. The size, location, and manufacturing services provided by each of our factories are set forth in the table below as of February 28, 2005.

Location	Approximate Factory Size (squarefeet)	Services
<i>Our Factories</i>		
<i>Korea</i>		
Seoul, Korea (K1)	670,000	Packaging services Package and process development
Pupyong, Korea (K3)	432,000	Packaging and test services
Kwangju, Korea (K4)	888,000	Packaging and test services
<i>Philippines</i>		
Muntinlupa, Philippines (P1) (1)	576,000	Packaging and test services Packaging and process development
Muntinlupa, Philippines (P2) (1)	152,000	Packaging services
Province of Laguna, Philippines (P3) (1)	400,000	Packaging services
Province of Laguna, Philippines (P4) (1)	225,000	Test services
<i>Taiwan</i>		
Lung Tan, Taiwan	335,000	Packaging and test services
Hsinchu, Taiwan	340,000	Packaging and test services
Hsinchu, Taiwan (2)	101,000	Wafer bump services
<i>China</i>		
Shanghai, China (3)	170,000	Packaging and test services
Shanghai, China (4)	930,000	Construction-in-process

Japan

Kitakami, Japan (3)	163,000	Packaging and test services
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Singapore

Kaki Bukit, Singapore (3)(5)	141,000	Test services
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United States

Wichita, Kansas (3)	30,000	Test services
Raleigh-Durham, NC (2)(3)	25,000	Wafer bump services

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- (1) As a result of foreign ownership restrictions in the Philippines, the land associated with our Philippine factories is leased from realty companies in which we own a 40% interest. Beginning July 1, 2003, these entities have been consolidated within the financial statements of Amkor, in accordance with FASB Interpretation No. 46. We own the buildings at our P1, P3 and P4 facilities and lease the buildings at our P2 facility from one of the aforementioned realty companies.
- (2) Property acquired in August 2004.
- (3) Leased facility.
- (4) Property acquired in May 2004 and is expected to house both packaging and test operations when completed. We do not anticipate that the property will be completed during 2005.
- (5) Property acquired in May 2004.

We believe that our existing properties are in good condition and suitable for the conduct of our business. At the end of fiscal 2004, we were productively utilizing the majority of the space in our facilities. We intend to expand our production capacity in 2005 and beyond as necessary to meet customer demand.

Our operational headquarters is located in Chandler, Arizona, and our principal executive office, which is leased, is located in West Chester, Pennsylvania. In addition to executive staff, the Chandler, Arizona campus houses sales and customer service for the southwest region, product management, finance, information systems, planning and marketing. During 2004, the West Chester location housed finance and accounting, legal, and information systems, and served as a satellite sales office for our eastern sales region. During 2005, the majority of the West Chester corporate functions will be transitioned to the Chandler, Arizona location, and as well to other locations, and thereafter the West Chester location will serve primarily as our principal executive office. Our marketing and sales office locations include sites in the U.S. (Chandler, Arizona; Irvine, Santa Clara and San Diego, California; Boston, Massachusetts; Greensboro, North Carolina; West Chester, Pennsylvania, and Austin and Dallas, Texas), Cayman Islands, China, France, Japan, Korea, the Philippines, Singapore, Taiwan and the United Kingdom.

Item 3. Legal Proceedings

We are currently a party to various legal proceedings, including those noted below. While we currently believe that the ultimate outcome of these proceedings, individually and in the aggregate, will not have a material adverse effect on our financial position or results of operations, litigation is subject to inherent uncertainties. If an unfavorable ruling were to occur, there exists the possibility of a material adverse impact on our net results in the period in which the ruling occurs. The estimate of the potential impact from the following legal proceedings on our financial position or overall results of operations could change in the future.

Epoxy Mold Compound Litigation

We have become party to an increased number of litigation matters relative to our historic levels. Much of our recent increase in litigation relates to an allegedly defective epoxy mold compound, formerly used in some of our packaging services, which is alleged to be responsible for certain semiconductor chip failures. In the case of each of these matters, we believe we have meritorious defenses, as well as valid third-party claims against Sumitomo Bakelite Co., Ltd. (Sumitomo Bakelite), the manufacturer of the challenged epoxy product, should the epoxy mold compound be found to be defective. We cannot be certain, however, that we will be able to recover any amount from Sumitomo Bakelite if we are held liable in these matters, or that any adverse result would not have a material impact upon us. Moreover, other customers of ours have made inquiries about the epoxy mold compound, which was widely used in

the semiconductor industry, and no assurance can be given that claims similar to those already asserted will not be made against us by other customers in the future.

Fujitsu Limited v. Cirrus Logic, Inc., et al.

On April 16, 2002, we were served with a third-party complaint in an action entitled Fujitsu Limited v. Cirrus Logic, Inc., No. 02-CV-01627 JW, pending in the United States District Court for the Northern District of California, San Jose Division. In this action, Fujitsu Limited (Fujitsu) alleges that semiconductor devices it purchased from Cirrus Logic, Inc. (Cirrus Logic) are defective in that a certain epoxy mold compound used in the manufacture of the chip causes a short circuit which renders Fujitsu disk drive products inoperable. Cirrus Logic, in response, denied the allegations of the complaint, counterclaimed against Fujitsu for unpaid invoices, and filed its third-party complaint against us alleging that any

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liability for chip defects should be assigned to us because we assembled the subject semiconductor devices. Upon receipt of Cirrus Logic's third-party complaint, we filed an answer denying all liability, and our own third-party complaint against Sumitomo Bakelite. Sumitomo Bakelite filed an answer denying liability. In June 2003, Fujitsu amended its complaint and added direct claims against us. In response, we filed an answer denying all liability to Fujitsu and amended our cross-claims against Sumitomo Bakelite to reflect Fujitsu's new claims against us. The parties engaged in extensive discovery activities. Fujitsu has indicated that it may seek damages in excess of \$100 million. In November 2003, Fujitsu filed an action against Cirrus Logic, Sumitomo Bakelite and us entitled *Fujitsu Limited v. Cirrus Logic, Inc., et al.*, Case No. 1-03-CV-009885, in the California Superior Court for the County of Santa Clara, based on facts and allegations substantially similar to those asserted in the Northern District Court of California. In December 2003, Cirrus Logic filed a cross-complaint against Sumitomo Bakelite and us in the Superior Court case, also based on facts and allegations substantially similar to those asserted in the Northern District Court case. By stipulation among the parties, the Northern District Court granted a stay of the action pending before it in favor of the action pending in the Santa Clara Superior Court, where discovery has continued. On March 29, 2004, we filed a motion to dismiss Fujitsu's amended complaint in the Superior Court. On April 2, 2004, we also filed a motion to dismiss Cirrus Logic's cross-complaint. The Superior Court held a hearing on our motions to dismiss on May 4, 2004 and granted dismissal of some of Fujitsu's and Cirrus Logic's claims against us. Fujitsu filed a second amended complaint in the Superior Court on or about June 18, 2004; Cirrus Logic filed a first amended cross-complaint on or about the same date. On July 19, 2004, we filed motions to dismiss certain claims asserted in the new complaints. At a hearing on August 24, 2004, the Superior Court denied our motion with respect to Fujitsu's claims, and granted our motion with respect to Cirrus Logic's claims. Cirrus Logic and Sumitomo Bakelite answered Fujitsu's second amended complaint on or about September 13 and 23, 2004, respectively, by generally denying all liability and asserting affirmative defenses. We filed a cross-complaint against Sumitomo Bakelite on October 1, 2004, asserting claims for breaches of warranties and indemnification; Sumitomo Bakelite filed an answer generally denying all liability and asserting affirmative defenses to our cross-complaint on or about November 1, 2004. We answered Fujitsu's second amended complaint on October 13, 2004, generally denying all liability and asserting affirmative defenses. On or about October 4, 2004, Cirrus Logic filed its second amended cross-complaint. We filed a motion to dismiss certain claims in Cirrus Logic's second amended cross-complaint on November 2, 2004; the Court denied our motion on November 23, 2004. Fujitsu answered Cirrus Logic's second amended cross-complaint on or about November 5, 2004 by denying liability and asserting affirmative defenses; Sumitomo did likewise on December 3, 2004, and we did likewise on December 10, 2004. On or about December 9, 2004, Cirrus Logic filed a motion for summary adjudication on its claims against Fujitsu; the Court denied Cirrus Logic's motion on March 1, 2005. On January 13, 2005, we filed motions for summary judgment and/or summary adjudication against Fujitsu's claims and certain of Cirrus Logic's claims against us. Sumitomo Bakelite filed motions for summary judgment and/or summary adjudication against Fujitsu's claims on or about January 13, 2005, and against Cirrus Logic's claims on or about February 10, 2005. The Court is scheduled to hear our and Sumitomo Bakelite's motions on March 29, 2005. Fact discovery formally closed on July 16, 2004, and the parties will complete what remains outstanding in the expected near term. Expert discovery is ongoing and currently scheduled to conclude by April 1, 2005. A trial in this matter is set to begin on May 2, 2005, and is estimated by the parties to last 20 to 60 court days. We intend to deny all liability, defend ourselves vigorously, pursue our cross-claims against Su